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LePix: monolithic pixel detector for LHC tracking systems

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Contents

Introduction

The typical layout of a hermetic detector at a collider experiment follows a standard design, covering as much as possible the volume around the interaction point. Particle identification procedures require momentum and energy measurements. Hence in such detectors we recognize three main components: an innermost tracking system for precise momentum measurements of charged particles, electromagnetic and hadronic calorimenters for energy measurements and external muon identification systems.

Every new generation of High Energy Physics (HEP) experiments or future upgrades of existing experiments require detailed $R\&D$ programs in order to explore and develop new technologies. It must be pointed out that the design and construction of such large systems involves a time scale of several years. In particular, the HEP community is already looking to new tracking and vertexing concepts and technologies suitable for the foreseen $\sim$ 2020 upgrades at the Large Hadron Collider (super-LHC, sLHC). These developments could be a benefit also for other future collider experiments as the International Linear Collider (ILC) and SuperB.
High luminosities, up to 10^{35} cm^{-2}s^{-1}, and high rates of p-p interactions at the sLHC will impose significant upgrades for inner tracking systems. More layers equipped with sensors featuring high granularity, speed and adequate radiation hardness will be required. Hence silicon pixel detectors will play an increasingly important role.
At present the standard approach for pixel detectors involves a so called *hybrid* technology, in which the sensor and its front-end electronics are developed separately and then connected with the bump-bonding technique.
The main limitations of hybrid pixel detectors are the material budget, the power consumption and the expensive production cost.
In perspective of the LHC upgrades and for future experiments new interesting silicon detectors for tracking and vertexing are under study and development.

The LePix project, which is the main topic of this work, is framed inside this context. In short, LePix (started in 2009) is a collaboration between CERN, INFN, IReS, Imperial College and C4i-MIND that explores the possibility of implementing monolithic pixel detectors in very deep submicron CMOS technology. In contrast with the hybrid approach, in a *monolithic* device both the sensor and the read-out electronics are integrated on the same silicon wafer. In a different way with respect to traditional monolithic sensors, in which the charge collection is driven by diffusion, the LePix key feature is the charge collection by drift. This is expected to improve both speed and radiation hardness. Hence the main challenge is to build the sensor and its electronics on a single reverse-biased substrate. The implementation of the front-end electronics using standard commercial microelectronics technologies reduces production cost. Thereby LePix is a long-term project potentially suitable for the LHC trackers upgrades and the next generation of HEP experiments.

In order to better understand general requirements for silicon tracking detectors in a high luminosity collider experiment, a description of the LHC harsh environment and of the Compact Muon Solenoid (CMS) inner tracking system is given in Chapter 1. Furthermore, a brief overview of the LHC upgrades scenarios is discussed.
In Chapter 2, both the hybrid and the monolithic architectures are compared. In particular, a description of the present layout of hybrid pixel detectors and the specifications of the CMS Silicon Pixel Tracker (SPT) provide an exhaustive background of present-day state of the art.
The LePix basic sensor concept and its front-end electronics schemes are presented in Chapter 3, whereas in Chapter 4 we discuss in more detail the prototype pixel matrices of the first 90 nm LePix submission.
Finally, in Chapter 5 we describe first tests and measurements performed with the experimental setup available in Turin since April 2011.

Chapter 1

Particle tracking in high luminosity environments

1.1 Silicon detectors for charged particle tracking

Precise and efficient tracking and vertexing procedures are essential in all HEP data analysis. A tracking system (tracker) provides measurements for different parameters. Particle hits measured closest to the interaction point are fundamental in determining the position of the primary vertex and of secondary vertices originated by the decays of short-living particles. The reconstruction of the tracks provides momentum measurements exploiting the curvature of charged particles trajectories in a magnetic field.
The pattern recognition, reconstruction of vertices and measurements of momentum and impact parameters of particles require therefore sensors featuring high spatial resolutions. Furthermore, some detectors provide also dE/dx measurements, essential in particle identification procedures.

These physics goals are achieved by using different detector technologies, each one with advantages and disadvantages. Thus, in a modern tracker we can recognize different sub-systems. An innermost region hosts vertex detectors, equipped with high granularity, fast and radiation tolerant sensors which exhibit a fine, two dimensional segmentation (mainly Silicon Pixel Detectors, SPD). Both solid state and gaseous sensors can be used in the central and outermost volume of the tracker, with a large variety of detector architectures available. Historically, gaseous Multi Wire Proportional Chambers (MWPC) and Drift Chambers (DC) have been employed for particle tracking in first collider experiments.
However, the last generation of HEP experiments has seen substantial progresses in the use of solid state detectors, and currently Silicon Strip Detectors (SSD) are widely used in all tracking systems, providing precise and efficient measurements of the trajectories of charged particles emerging from

the interaction region. Hence innermost layers of SPD and external layers of SSD arranged in a barrel geometry represent a standard configuration for a silicon tracker in a high luminosity and high energy collider experiment. In these systems a huge density of sensitive elements is employed, leading to a very large number of read-out channels and several thousands of detecting modules. Besides this standard solution, some experiments (mainly inside the heavy-ions community) have been instrumented also with Silicon Drift Detectors (SDD) and gaseous Time Projection Chamber (TPC).

Several years of *R&D* studies have demonstrated that silicon sensors equipped with Very Large Scale Integration (VLSI) front-end electronics can provide precise and efficient measurements for charged particle tracking in a high luminosity environment. [1]
At first, silicon detectors offer high spatial resolutions ($\geq$ 5 μm) and maximum granularity, therefore can cope with huge track densities. Sensors in which the charge collection is driven by drift exhibit fast response ($\geq$ 10 ns) and adequate radiation hardness. In addition, good energy resolutions can be obtained with a very low amount of material. In particular, the stopping power for a MIP is $\sim$ 390 eV/μm. This leads to about 32'000 electron/hole pairs in 300 μm of thickness due to the low silicon ionising energy (3.6 eV). Typically no charge amplification is performed in the sensor. At the same time, a particle hit can be measured with no appreciable effect for the particle itself, because the energy loss is small ($\sim$ 0.1 MeV in 300 μm) and the low material budget minimizes Multiple Coulomb Scattering effects. However, maintaining good signal-to-noise ratios in hostile radiation environments requires low operating temperatures, in order to keep leakage currents at an accettable level. Finally, silicon exhibits excellent mechanical properties and low production cost.
Silicon detectors for particle tracking require radiation-hard and high specialized read-out integrated circuits. The radiation tolerance is of particular importance for pixel detectors at radii very close to the interaction point, where the front-end electronics receive the highest radiation doses. These circuits are implemeted in VLSI technologies.
In particular, the development of a read-out chip with adequate performance involves long-term projects, with a typical man-power of 5$\div$10 man-years. Each prototype requires preliminary studies of the architectures, simulations performed with professional CAD softwares, layout design and experimental tests.

In order to better understand specifications and performance requirements of a silicon tracking system for a high luminosity experiment, we describe the extreme operating conditions at the CERN Large Hadron Col-

lider (LHC). Moreover, a general overview of the Compact Muon Solenoid (CMS) tracker (at present the largest full-silicon tracker ever built) provides an exhaustive and detailed example of the nowaday state of the art for silicon tracking systems [2]. Of course, according to the aim of this work, for our future considerations we will gradually focus the attention on silicon pixel detectors only.

1.2 High luminosity environments at the LHC

Performance and general requirements for a silicon tracking system in a high luminosity environment at the LHC are challenging.
As a matter of fact, ATLAS and CMS have been designed as general purpose high luminosity experiments to explore particle physics at the TeV energy scale, exploiting unprecedented opportunities offered by the LHC machine. The accelerator has been designed to deliver both proton-proton and lead ions collisions. In particular, the LHC provides p-p interactions at nominal $\sqrt{s} = 14$ TeV (7 TeV/beam) and luminosities up to 10^{34} cm^{-2} s^{-1}, with a design 25 ns bunch crossing. However, nowaday LHC operating conditions for the first 2010-2012 low luminosity pilot physics run are different with respect to nominal ones. At the time of writing the machine is delivering p-p collisions at $\sqrt{s} = 7$ TeV with a luminosity $\sim 3 \times 10^{33}$ cm^{-2} s^{-1}. Moreover, the bunch spacing is 50 ns.

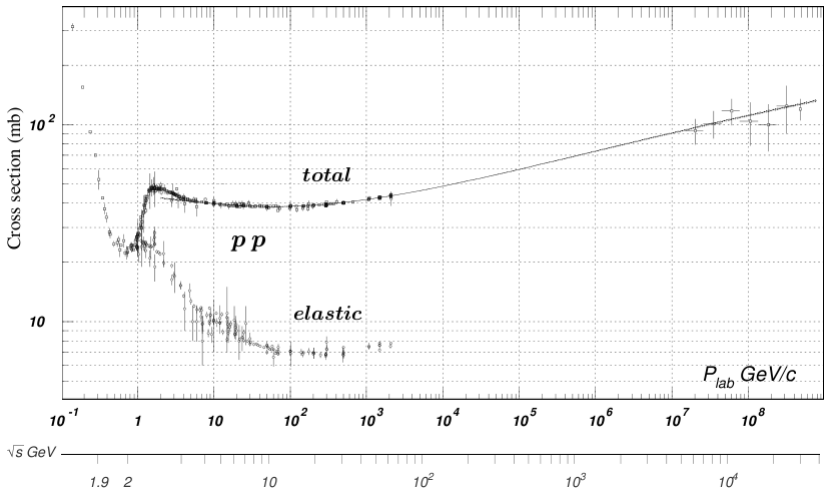

Figure 1.1: Total and elastic cross section for p-p collisions as a function of laboratory beam momentum and total center-of-mass energy [3].

High luminosities and high center-of-mass energies in a hadron collider are fundamental in order to *discovery* new physics processes with predicted small cross sections. Unfortunately, this leads to a overwhelming background rate compared to the expected interesting physics events.
As shown in Figure 1.1, the total p-p cross section at the $\sqrt{s} = 14$ TeV energy scale is expected to be roughtly 100 mb. This implies an extimated total interaction rate of approximately 10^9 inelastic events/s at the design 10^{34} cm^{-2} s^{-1} LHC luminosity.

On the other hand, interesting physics processes have a cross sections orders of magnitude smaller than the total inelastic one. For instance, in Figure 1.2 are depicted the main Standard Model processes which can contribute to the Higgs boson production in a hard p-p collision. As shown in Figure 1.3 respective typical cross sections at $\sqrt{s} = 7$ TeV are of the order of pb, increasing with the center-of-mass energy. Note that even if the dominant process on the whole M_H spectrum is the gluon-gluon fusion via a t-quark loop (with about 10 pb, increasing to about 50 pb at $\sqrt{s} = 14$ TeV) other processes (e.g. WW and ZZ fusion or Higgs-strahlung) which have smaller cross sections can have a better signature. Once produced, the Higgs particle should immediately decay with a wide range of decay channels depending on its mass M_H. Typical predicted branching ratios (BR) as a function of M_H are depicted in Figure 1.4.
The expected number of Higgs events for a certain decay channel is given therefore by the relationship $N_H = L_{int}\, \sigma\,(\sqrt{s}\,)\; BR\,(M_H)$. The importance of a high luminosity and high center-of-mass energy environment arises from this general result. The cross section increases with $\sqrt{s}$, whereas the total p-p cross section remains almost constant. The statistics increases with the integrated luminosity recorded by the experiment. As a matter of fact, the integrated luminosity becomes a fundamental parameter of the experiment itself. However, we can immediately recognize that the ratio between cross sections is $\sigma_H/\sigma_{TOT} \sim 10^{-7} \div 10^{-8}$. Hence as already mentioned most of the created p-p events do not contain any interesting physical signatures, but add up to a huge background of particles (*minimum bias*).
At the design luminosity it is expected that a mean of 20 inelastic collisions superimposes on a event of interest, creating $\sim 10^3$ charged particles from the interaction region every 25 ns.

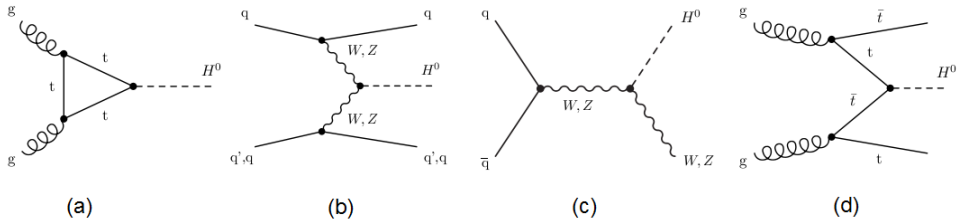

Figure 1.2: Higgs boson production mechanisms in p-p collisions: gg fusion (a), W/Z fusion (b), Higgs-strahlung (c) and $t\bar{t}$ associated production (d).

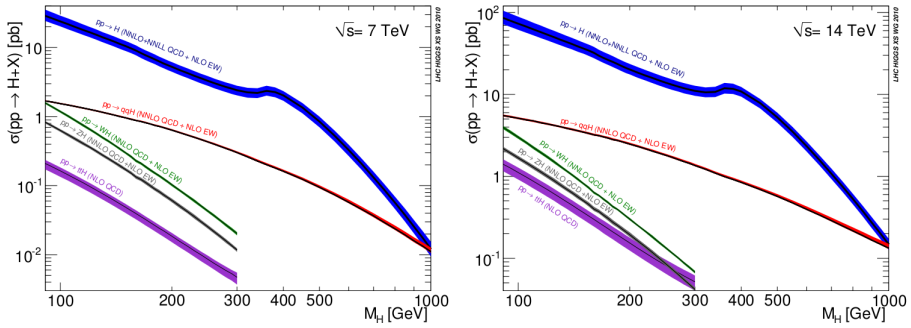

Figure 1.3: Predicted Higgs boson production cross sections in p-p collisions at $\sqrt{s} = 7$ TeV (left) and 14 TeV (right) as a function of the mass M_H [4].

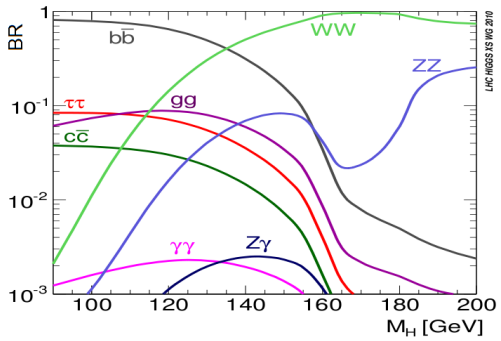

Figure 1.4: Predicted Higgs boson branching ratios for different decay channels as a funtion of the mass M_H [4].

This overwhelming background of charged particles requires a very careful design of the tracking system, introducing severe constraints and technological challenges.
The spatial resolution is clearly the first important parameter in order to cope with the huge track density. On the other hand, the on-line event selection process must reduce the interactions rate to about 100 events/s for storage and subsequent analysis, with at least a 10^7 suppression factor. In particular, the short time interval between two collisions require detectors and front-end electronics with fast time response (< 25 ns), in order to minimize pile-up effects.
Moreover, the large flux of particles coming from the interaction region leads to an extremely hostile radiation environment, requiring both radiation-hard detectors and front-end electronics. Note that this aspect represents a crucial issue for all hadron colliders, in which high luminositiy p-p or p-$\bar{p}$ interactions generate high charged particle fluences. In a e^+e^- experiment with the same discovery potential this problem is orders of magnitude smaller.

As a matter of fact, a full-silicon based tracking system can meet these extreme requirements and cope with the LHC hostile environment.

1.3 The CMS apparatus at the LHC

A perspective view of the CMS detector is shown in Figure 1.5, completed with a transverse view in Figure 1.6. We can immediately recognize the standard configuration of a modern hermetic particle detector for a collider experiment. The basic layout involves an innermost full-silicon based tracking system surrounded by electromagnetic and hadronic calorimenters and external muon detectors. Being CMS a general-purpose experiment, the apparatus has been designed in order to satisfey all the specific requirements of its wide physics programme.

A key aspect in the detector design is the choice of a solenoidal configuration of the magnetic field for momentum measurements, using a 4 T superconducting solenoid. The dimensions of the magnet are 13 m of length times 5.9 m of inner diameter. As a result of this choice, the CMS apparatus exhibits a very compact barrel layout, accomodating the inner tracking system and the calorimetry inside the bore of the magnet coil, improving therefore the detection and energy measurement of electrons and photons. Furthermore, the iron return yoke of the magnet is large enough to host the external muon identification system.

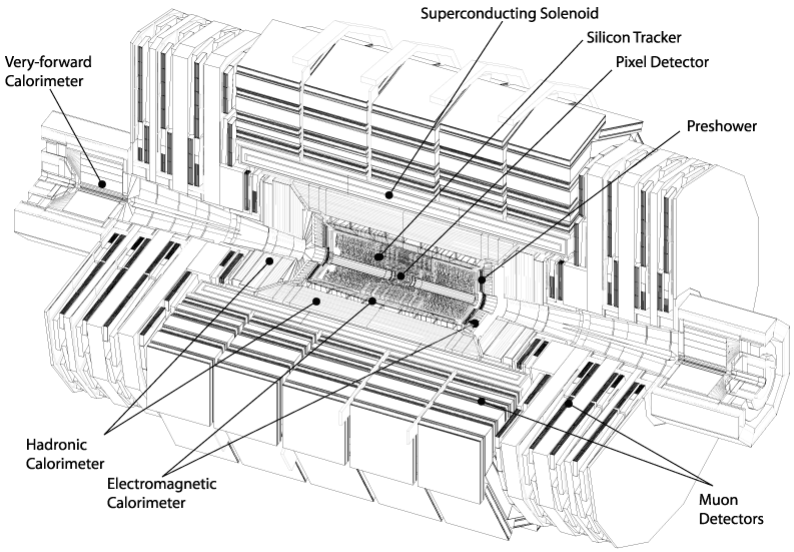

Figure 1.5: CMS detector - perspective view.

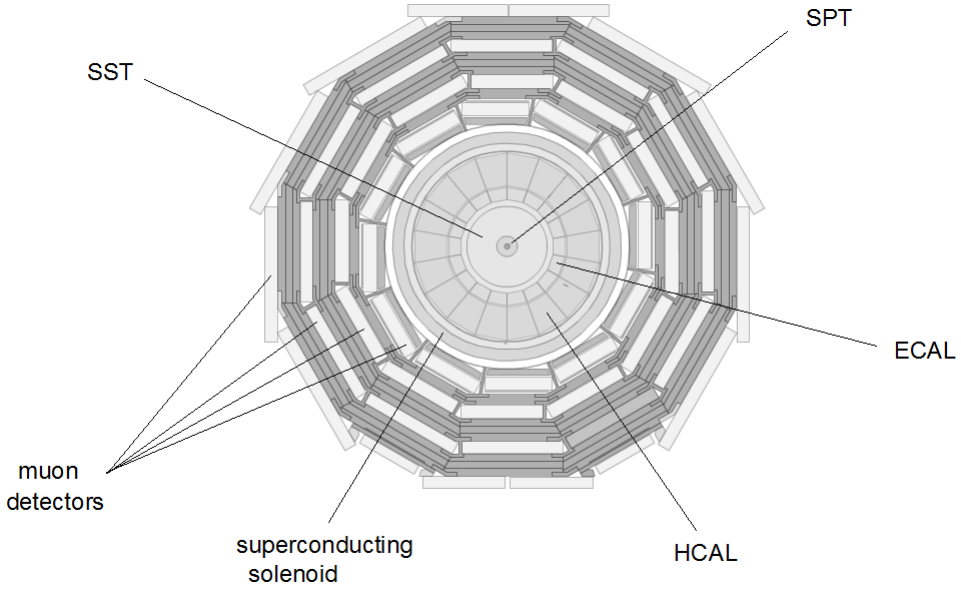

Figure 1.6: CMS detector - transverse view.

The overall dimensions of the detector are 21.6 m of length times 14.6 m of diameter, with a total weight of 12'500 tons.
The sensitive volume ensures a full geometric coverage up to $|\eta| < 5$, essential for a good transverse missing energy and di-jet mass resolution.
Remind that in this context the geometric coverage is given in terms of the pseudorapidity $\eta = -\ln[\tan\theta/2]$, where θ is the angle between the particle momentum and the z axis along the beam direction.

The tracking volume is a cylinder of 5.8 m of length and 2.6 m of diameter inside the strong 4 T magnetic field, composed of 3 barrel layers close to the interaction region equipped with *hybrid pixel detectors*, surrounded by 10 barrel layers of *silicon microstrip*. Furthermore, specific endcaps disks on each side ensure a forward/backward coverage up to $|\eta| < 2.5$.

The electromagnetic calorimeter (ECAL) uses lead tungstate ($PbWO_4$) crystals providing a good energy resolution with coverage up to $|\eta| < 3$. The scintillation light is detected by silicon avalanche photodiodes (APD) in the barrel region and vacuum phototriodes in the endcap region. A preshower for π^0 rejection is installed in front of the endcap ECAL.
The ECAL is then surrounded by a brass/scintillator sampling hadronic calorimeter (HCAL) complemented by a very forward calorimenter which extends the coverage up to $|\eta| < 3$. The scintillation light is converted by using wavelenght-shift optical fibres, then is detected by hybrid photodiodes (HPD). Moreover, a coverage up to $|\eta| < 5$ is provided by an iron/quartz fiber calorimeter, which Cherenkov light is detected by standard photomultipliers (PMT). A large geometric coverage in this case becomes essential for good missing energy and di-jet mass resolution.

Finally, the outermost volume of the apparatus hosts a muon spectrometer, composed by 4 stations of aluminium drift tubes (DT) in the barrel region and cathode strip chambers (CSC) in the endcap region, both complemented by resistive plate chambers (RPC).

1.4 The CMS tracking system

As already mentioned, the operating conditions for a tracking system at the LHC are very challenging. At the design luminosity of 10^{34} cm^{-2} s^{-1} the machine will provide about 10^9 interactions/s creating on average 10^3 charged particles every 25 ns. The intense particle flux leads to a very hostile radiation environment, requiring both radiation-hard detectors and front-end electronics.
On the other hand, the expected CMS physics program requires excellent tracking and vertexing performance. In particular, efficient and precise reconstruction of charged particles tracks with transverse momentum p_T above 1 GeV in the pseudo-rapidity range of $|\eta| < 2.5$ are of primary importance. Moreover, precise measurements of secondary vertices and impact parameters are fundamental in the identification of heavy-flavors quarks which are produced in many of interesting physics channels. Furthermore, in order to reduce the huge event rate to about 100 Hz (which can be permanently stored), the tracking information is heavily used in the CMS on-line event selection process.

A schematic cross section of the overall CMS tracking system is shown in Figure 1.7.

The tracker is composed of a silicon pixel tracker (SPT) and a silicon strip tracker (SST). The SPT is a system of 3 barrel layers equipped with *hybrid pixel detectors* at radii 4.4 cm, 7.3 cm and 10.2 cm, close to the beryllium beam pipe (of radius 2.9 cm). A more detailed description of the CMS vertex pixel detector specifications is given in Chapter 2.
The region between 20 cm of radius and 116 cm is occupied instead by the SST, which is composed of 10 barrel layers of silicon microstrip detectors. Each layer is then completed by end-caps on each side of the barrel, consisting of 2 disks in the pixel tracker and 3 plus 9 disks in the strip tracker.
Furthermore, in the SST we can recognize two different sub-systems, a Tracker Inner Barrel (TIB) and a Tracker Outer Barrel (TOB). The TIB extends in radius towards 55 cm and $|z| < 65$ cm. It's composed of 4 barrel layers supplemented by 3 end-caps disks at each end, i.e the Tracker Inner Disks (TID). The TIB system is then surrounded by the TOB, which consists of 6 barrel layers completed by 9 lateral disks, i.e. the Tracker End Caps (TEC).

The total acceptance in pseudorapidity is $|\eta| < 2.5$ and this tracking layout ensures at least 2 hits in the SPT and $8 \div 9$ hits in the SST.

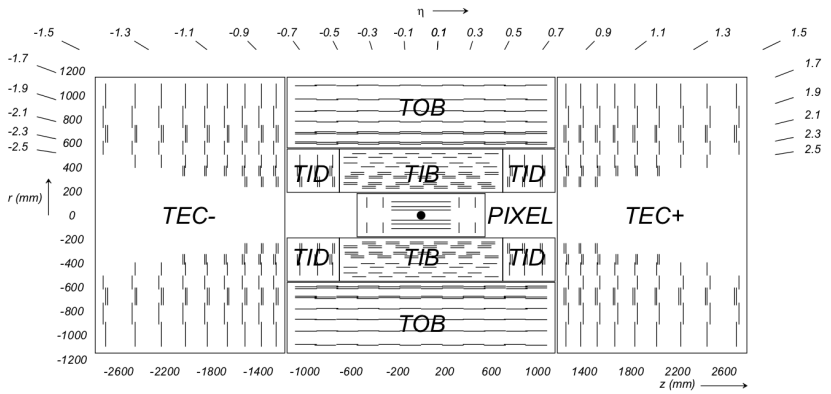

Figure 1.7: Schematic cross section of the CMS tracking system (each line represents a detector module).

Pitch and thickness of the strips depend on the layer, because the hit rate density decreases with the radius, from 1 MHz/mm^2 at radius 4 cm to 3 kHz/mm^2 at radius 115 cm. Hence the TIB uses silicon sensors with a thickness of 320 μm and a pitch strip which varies from 80 to 120 μm. Since the radiation levels are smaller in the TOB region, ticker and wider sensor are used there, with 500 μm of thickness and 120 to 180 μm of pitch.
With a total active silicon area of about 200 m^2, the CMS tracker is the largest silicon tracker ever built, with 1440 pixel-modules and 15'148 strip modules, corresponding to 66 million pixels and 9.3 million silicon strips.

In order to increase the radiation tolerance and minimize the noise, the whole tracker volume needs to be cooled to a low operating temperature. This introduces a challenging constraint, because it is in conflict with the proper electromagnetic calorimeter operating conditions, that require good temperature stability in the (18 $\pm$ 4) °C range. In particular, starting with a cooling temperature slightly below -10 °C, after 10 years of operation it is expected that this value will have to decrease to about -27 °C in order to suppress the foreseen increased leakage currents. Hence, all structures in the tracker have to survive temperature cycles between the room temperature and about -30 °C.

Both pixels and microstrips front-end electronics have been fabricated in standard 0.25 μm CMOS technology.

1.5 LHC upgrades scenarios

Despite present-day LHC operating conditions do not reach yet the nominal values, activities focusing on the upgrades of the LHC detectors have already started. This is necessary since the typical time required for designing and building such large systems is of the order of 10 years. Therefore first *R&D* programs must start now in order to be ready for $\sim$ 2020, when new detectors will be required to exploit the full potential of the machine.
As a matter of fact, several upgrades scenarios have been studied since the LHC design phase, following the expected evolution of the machine performance and involving both short-term and long-term plans in the forthcoming 10 years. A recent 2011-2021 CERN draft plan has been proposed in March 2011 and is shown in Figure 1.8.
The aim of this section is to compare the currently operating conditions of the LHC machine with its expected short-term and long-term evolution perspectives.

As already mentioned, at the time of writing the accelerator is delivering two beams of protons colliding at $\sqrt{s} = 7$ TeV with an instantaneous luminosity $\sim 10^{33}$ cm^{-2} s^{-1} and a 50 ns bunch crossing.
In Figure 1.9 is shown the total integrated luminosity delivered and recorded by CMS between March and September 2011 under these LHC operating conditions, which exceeds 2.5 fb^{-1}. LHC operating conditions for 2012 are under consideration both for the center-of-mass energy and for the bunch spacing. The first 2010-2012 physics run represents the *phase-0* of the LHC commissioning.

A first long shutdown (LS1) is foreseen in 2013 (about 16$\div$18 months). It will be mainly a technical shutdown, in order to reach ultimate nominal performance with minimum machine and detectors hardware modifications. ALICE, ATLAS and CMS plan to change and reduce the beam pipe (from 29 mm of radius to 25 mm). Most important, with an energy upgrade the center-of-mass energy should be increased to nominal 14 TeV. After the LS1 the LHC will enter in the *phase-I*.
A second long shutdown (LS2) is planned instead for 2017-2018, involving first major hardware modifications in order to increase the LHC luminosity by one order of magnitude, up to 2×10^{34} cm^{-2} s^{-1} before 2020. Hence interaction regions ad RF upgrades will be performed. These new LHC operating conditions will require also trackers upgrades in ATLAS and CMS. Pixel detectors and front-end electronics in the innermost layers have been designed more than 10 years ago to operate with a maximum luminosity of 10^{34} cm^{-2} s^{-1}.

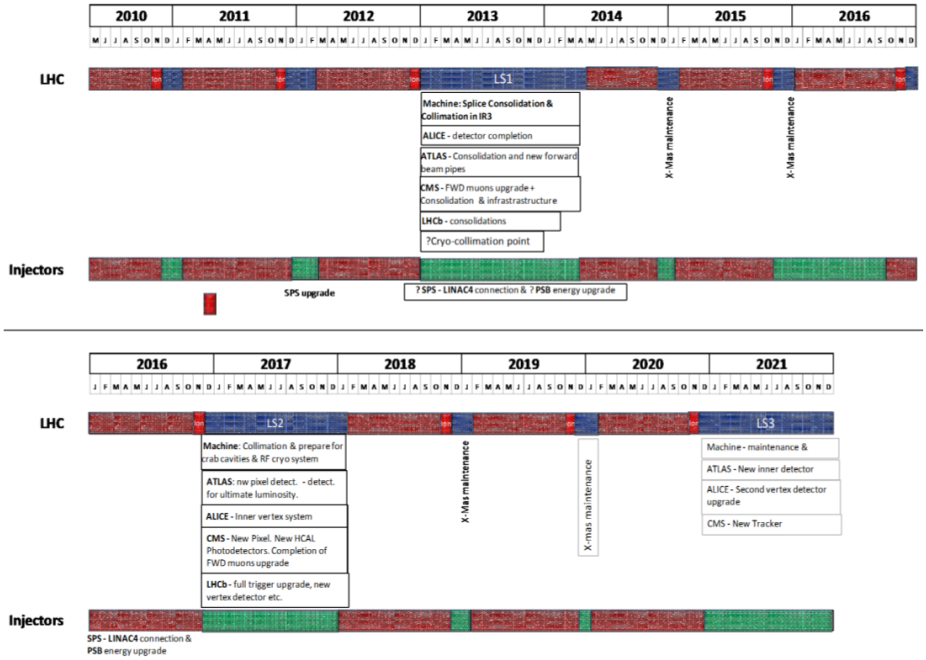

Figure 1.8: March 2011 CERN draft plan for the LHC upgrades scenarios [5].

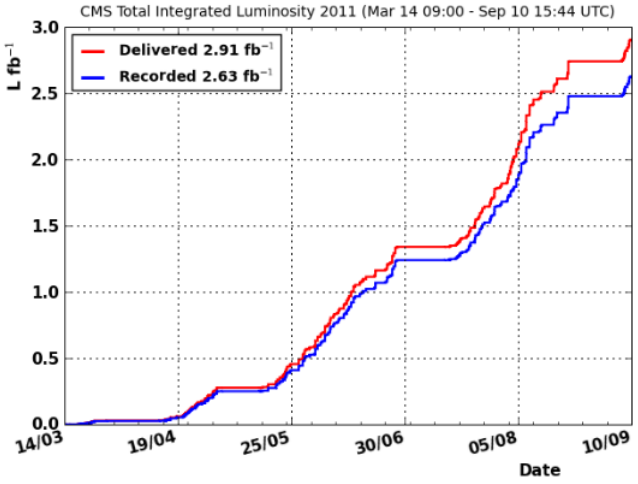

Figure 1.9: Total integrated luminosity delivered and recorded by CMS between March and September 2011.

For instance, first $2 \div 3$ % of data losses in the present CMS pixel read-out chip (designed in 1998) will start becoming evident at 10^{34} cm^{-2} s^{-1} in the innermost layer. An unaccetable ~ 15 % of data losses is expected running at 2×10^{34} cm^{-2} s^{-1}, leading to a major degradation of vertexing performance. Under these conditions the ability of the experiments to continue to deliver physics benefiting of the high luminosity environment provided by the LHC will be seriously compromised.
Thus, first *R&D* programs for a 2017 trackers upgrade have been started, in order to guarantee adequate vertexing and tracking performance until the end of the *phase-I*. For instance, the 3 innermost layers equipped with hybrid pixel detectors in CMS will be replaced due to radiation damage and an additional fourth pixel layer close to the beam pipe is under consideration. After the LS2 upgradres LHC is planned to deliver an integrated luminosity of about $300 \div 700$ fb^{-1} before the end of 2020, increasing physics oppotunities.

At the end of first 10 years of LHC operating, a third long shutdown (LS3) in 2021 will increase the luminosity up to 10^{35}cm^{-2}s^{-1} upgrading LHC to Super-LHC (sLHC) in the so called *phase-II*. Of course this perspective involves long-term upgrade scenarios. Important modifications to the LHC ring magnets and to the injectors will be required. The replacement of the entire ALICE, ATLAS and CMS tracking systems will be performed, introducing more layers equipped with sensors featuring high granularity, speed and adequate radiation hardness. As a matter of fact, silicon pixel detectors will be required also in regions at present instrumented with conventional silicon strips.

Hence, new solutions with respect to the present-day state of the art for vertex detectors will be required. In this perspective, very interesting and alternative architectures are offered by the *monolithic* approach.

Chapter 2

Hybrid and monolithic architectures for silicon pixel detectors

2.1 Present standard layout of pixel detectors for particle tracking

In this section the main features of *hybrid pixel detectors* are discussed. The basic building block of a pixel cell is sketched in Figure 2.1.
The sensitive element is a reverse biased junction formed by a lightly doped substrate and a collection electrode. A ionizing particle that crosses the sensor generates electron/hole pairs that move in the depletion region under the action of the electric field. Hence the charge collection is driven by drift, providing fast response and increasing the radiation tolerance. As known, the thickness of the depletion region is determined by the doping levels and the reverse bias voltage.

The key word in this context is *hybrid*, which means that sensor and front-end electronics are fabricated separately on different silicon wafers and then mated. In particular, as shown in Figure 2.2 each pixel cell is connected to its own specific read-out electronics by using the *bump bonding* technique. A tiny ball of conducting solder (tipically indium or Pb-Sn) is deposited onto a special pad. Hence the read-out chip and the pixelated surface are put in contact and glued together face to face by using the flip-chip technology.

For the sake of completeness we can mention that also silicon strip detectors exhibit a separation between the sensor and its front-end electronics,

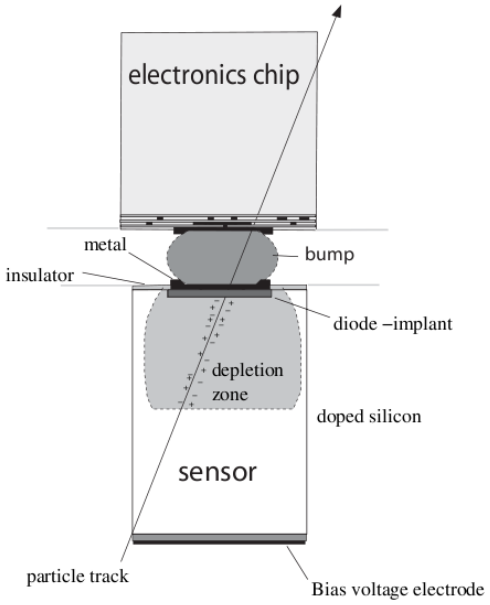

Figure 2.1: Schematic view of a hybrid pixel detector basic building block. [6]

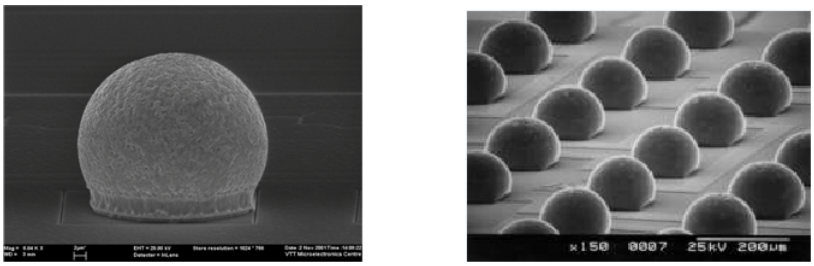

Figure 2.2: Solder bumps.

which are connected by using the *wire-bonding* technology instead.

Hibrid pixel detectors with performance adequate for the LHC hostile environment pose several challenges. On the one hand, each pixel cell needs a sophisticated read-out circuitry, demanding the use of VLSI technologies. On the other hand, the large number of channels requires high interconnection densities, provided by the bump bonding technique, which dominates the production cost. Hybrid pixel detectors are therefore expensive devices. This cost can be afforded only in the innermost 2-3 layers (and relative end disks) of a collider tracking system, very close to the interaction region. However, as already mentioned, at present there are no satisfactory alternatives to hybrid pixel detectors, which for the state of the art represent *the* standard approach for fast and radiation tolerant pixel sensors adequate for high luminosity experiments.

2.2 CMS Silicon Pixel Tracker specifications

All of the LHC collider-experiments (ALICE, ATLAS, CMS, LHCb) as well as other fixed target experiments employ hybrid pixel detectors in the innermost region of trackers, covering areas $\sim$ m^2.
Here a more detailed description of the CMS Silicon Pixel Tracker (SPT) is given. In particular, both the architecture of a pixel detector module and the radiation environment close to the interaction region are discussed.

A schematic view of the overall SPT is shown in Figure 2.3. The system consists of 3 barrel layers plus 2 end-cap disks on each side. The length of each barrel layer is 53 cm and radii are 4.4, 7.3 and 10.2 cm. Note that the volume of the SPT is much smaller with respect to the SST one, that occupies instead the remaining radial region between 20 cm and 116 cm with an overall length of 5.8 m. As shown in Figure 2.4 this layout provides at least 2 hits over almost the full pseudorapidity range $|\eta| < 2.5$ with a maximum spatial resolution of 10 μm in $r\phi$ and 20 μm in z.
Both the barrel layers and the end-cap disks are composed of pixel detector modules.

The complete structure of a barrel layer pixel detector module is shown in Figure 2.5. The overall dimensions are 66.6 mm $\times$ 26 mm.

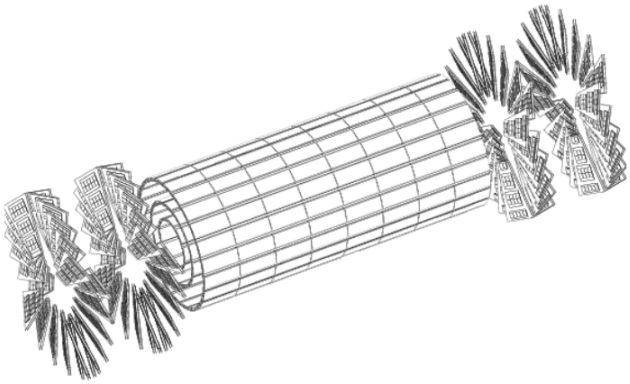

Figure 2.3: Overall layout of the CMS Silicon Pixel Tracker (SPT).

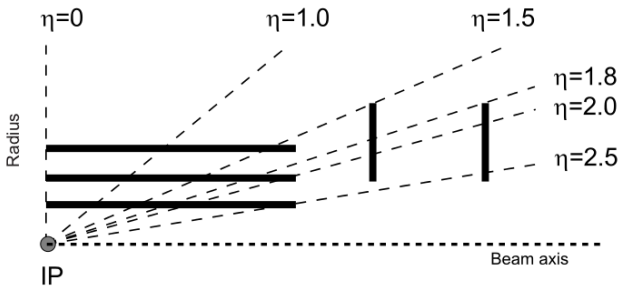

Figure 2.4: A schematic illustration of the SPT. This layout provides at least 2 hits over almost the full pseudorapidity range $|\eta| < 2.5$.

Two basestrips made of 250 μm thick silicon nitride provide the mechanical support for the entire module. The sensitive layer has an active surface of 64 mm $\times$ 16 mm, with a thickness of 250 μm. It contains 8 or 16 pixel matrices (depending upon the barrel layer radius) with 52 $\times$ 80 pixels each one. The pixel size is 100 μm $\times$ 150 μm, whereas the nominal reverse bias is 300 V. The front-end electronics consists therefore of 8 or 16 read-out chips (ROCs) bump-bonded to the sensitive silicon layer. In particular, each single ROC is a full custom Application Specific Integrated Circuit (ASIC) fabricated in standard 0.25 μm CMOS technology. Each ROC provides amplification, shaping and buffering of the charge signal from the sensor with a 40 MHz serial read-out. In order to reduce the data rate, a zero suppression is performed with an adjustable threshold for each pixel.
The High Density Interconnect (HDI) forms the upper part of the module with a flexible and low mass printed circuit board (PCB) which distributes signals and power to the electronics. Furthermore, the center of the HDI hosts the Token Bit Manager (TBM) chip, which controls the read-out procedure of the ROCs group. Each signal from the TBM encodes a pixel hit by using six values. Five values are used for the pixel address (i.e. row and column of the pixel in the matrix and the respective ROC identify number). The sixth value represents the charge signal. Note that only the charge signal is truly analog. Address values are instead discrete levels generated by DACs.

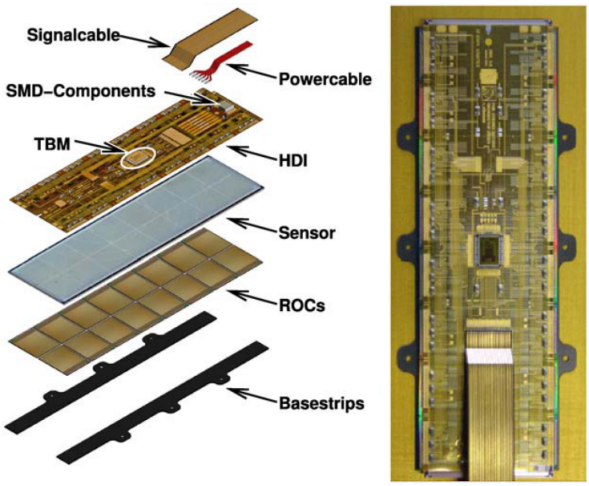

Figure 2.5: Overall layout of a barrel pixel detector module.

The power budget depends on the pixel hit rate. At the LHC design luminosity of 10^{34} cm^{-2} s^{-1} each ROC should contribute with 34 μW per

pixel, leading to a total power consumption of the order of 250 mW/cm^2. This parameter will become a severe constraint for any tracker upgrade plan. The overall Silicon Pixel Tracker covers an active area of about 1 m^2 and contains 1440 detecting modules, corresponding to 15'840 ROCs and 66 million pixels.

Without doubt, the harsh radiation environment in which the CMS pixel tracker have to work is a challenge. As already mentioned, each LHC bunch crossing at the design luminosity creates on average 10^3 charged particles from the interaction point. This leads to a hit rate density of 1 MHz/mm^2 at a radius of 4 cm, falling to 60 kHz/mm^2 at a radius of 22 cm and 3 kHz/mm^2 at 115 cm.

Table 2.1 shows the expected hadron fluences and radiation levels in different radial layers of the CMS tracker (barrel region) for an integrated luminosity of 500 fb^{-1}, corresponding to roughtly 10 years of LHC operation.

radius [cm]	charged particle flux [cm^{-2} s^{-1}]	dose [kGy]	fluence of fast hadrons [$\times 10^{14}$cm^{-2}]
4	10^8	840	32
11		190	4.6
22	6×10^6	70	1.6
75		7	0.3
115	3×10^5	1.8	0.2

Table 2.1: CMS tracker radiation levels in different radial layers [2].

All tests have been shown that the Silicon Strip Tracker will remain fully operational for an expected lifetime of 10 years. In the Silicon Pixel Tracker instead, which has to survive to higher radiation doses, the innermost layer at radius 4.4 cm is foreseen to stay operational for at least 2 years at the nominal LHC luminosity.
The particle detection inefficiency has been measured with a high-rate pion beam and reaches 0.8 %, 1.2 % and 3.8 % respectively for the three barrel layers of the SPT at a luminosity of 10^{34} cm^{-2}s^{-1}.
Furthermore, the front-end electronics of the ROC has been designed for a maximum luminosity of 1×10^{34} cm^{-2} s^{-1}, corresponding to a particle flux of 40 MHz cm^{-2} at 4.3 cm inner radius.

2.3 The monolithic approach

Silicon strip and hybrid pixel detectors are mature technologies, successfully employed in almost every collider experiment in high energy physics. Beside these standard architectures, additional interesting silicon detector structures are under study and development in perspective of the LHC upgrades and for future experiments.

One of the most promising alternatives to the hybrid architecture is the *monolithic* approach. In hybrid pixel detectors the sensor and its front-end electronics are developed separately. In a monolithic device, in contrast, both the detector and the read-out electronics are *integrated* on the same silicon wafer. Hence the new challenge becomes to build the sensor and its processing electronics on a single substrate.

The first monolithic pixel detector successfully operated in a particle beam was made in 1992. Present approaches which work in this direction are for example the Monolithic Active Pixel Sensors (MAPS) and the Depleted Field Effect (DEPFET) detectors.

In the next section a description of MAPS is given, which represent a necessary step in order to understand the LePix project.

2.4 Monolithic Active Pixel Sensors (MAPS)

Monolithic Active Pixel Sensors (MAPS) were invented in the early '90s for the detection of visible light. However at the beginning the relatively poor performance limited their use to some specific applications (e.g. cameras) as imaging devices only. The use of MAPS as detectors for particle physics was first proposed at the end of 1999 instead, after continuous improvements in the technology.

In its simplest form, the pixel architecture of a MAPS is sketched in Figure 2.6. The basic idea essentially is to integrate the first transistor of the read-out electronics chain on the detector surface itself. The remaining electronics is built at the periphery, embedded on the same piece of silicon. As shown in Figure 2.6, the sensitive volume is a thin ($\approx 15 \div 30\ \mu$m) lightly doped p^- epitaxial layer between a p^{++} substrate and a p^+ well. The charge collecting element is a n-well implant in contact with the sensitive layer.

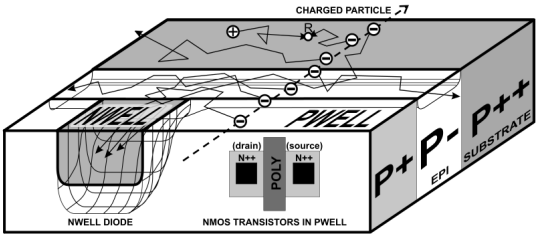

Figure 2.6: Sketch of a MAPS structure [7].

The high difference in doping concentrations (about three orders of magnitude) between the p-well, the p^{++} substrate and the p^{-} epitaxial layer generates an intrinsic electrostatic potential. The two external layers act as reflective barriers. Differently from hybrid pixel detectors, there is no reverse bias applied and the electrical potential arises only from the difference in doping concentrations. Electrons originated by the passage of an ionizing particle ($\approx$ 80 electron/hole pairs per μm for a MIP) migrate *by thermal diffusion* towards the n-well collecting electrode, mainly confined within the epitaxial layer by the above-metioned electrostatic barrier. Hence the charge collection on the n-well is fully dominated by diffusion.
According to the monolithic approach a transistor is built in the p-well itself, which represents the first device of the front-end electronics chain. The parasitic capacitance of the collecting electrode provides the charge to voltage convertion and the output signal drives the gate of the transistor.
The remaining read-out electronics is integrated at the periphery of the sensitive area and is developed in *standard* CMOS technology. This is a MAPS key feature, because standard CMOS processes are *commercially* available. As a matter of fact, MAPS differ from previously proposed monolithic devices in particular for using standard CMOS processes.

This pixel architecture offer advantages and disadvantages. The monolithic approach provides a very compact detector, with a very low material budget (a few tens of μm of thickness) and low production cost due to the implementation in standard CMOS technologies. Furthermore, MAPS exhibit a low power consumption (a few tens of mW/cm^2).
On the other hand, the duration of the charge collection by diffusion (of the order of 100 ns) increases recombination and trapping probabilities in the epitaxial layer. Therefore MAPS are relatively slow devices and more sensitive to radiation damage with respect to standard hybrid pixel detectors. Moreover, in order to obtain a good signal-to-noise ratio the pixel capacitance must be minimized. Hence the area of the collecting electrode must be kept to a minimum. For this reason only NMOS transistors can be integrated around the collection electrode, built on the p-well, whereas the n-well surface is too small to host a PMOS device. This disadvantage imposes severe

limitations for the circuitry integrated in the sensor. Typically the output voltage is fed to a single transistor in source follower (SF) configuration or to a single-stage amplifier composed of two devices with a maximum voltage gain ≈ 10. Furthermore, no local storage of particle hits can be performed. Therefore MAPS usually employ serial read-out schemes such as the *rolling shutter* technique.

Good performance in charged particle detection have been obtained with the MIMOSA (Minimum Ionising MOS Active Pixel Sensor) chips. This is a family of several MAPS prototypes which explore different CMOS technologies and pixel optimizations. Nevertheless a monolithic pixel detector with performance adequate for a hostile environment such as the LHC one is a challenge for the nowaday state of the art.

2.5 The LePix project

The LePix project was conceived in 2009 framed inside the wide scenarios of the LHC upgrades. It represents a long-term $R\&D$ project potentially suitable for the *phase-II* of the LHC upgrades and for future HEP experiments. The first article [8] was published in March 2010, finalizing at the same time the first submission with the foundry.
In this section a general overview of the project is given, describing in more detail the sensor concept in Chapter 3.

Increasing the LHC luminosity pixel detectors will be required also in tracker regions at present covered by silicon strip detectors. However the power consumption and production cost will not increase.
As previously discussed MAPS exhibit a low power consumption and require a low material budget, integrating the sensor and its read-out electronics on the same substrate. Due to the charge collection by thermal diffusion, MAPS are slow and more sensitive to radiation damage.
On the other hand, in hybrid pixel detetectors the charge collection by drift ensures high speed and adequate radiation tolerance. The main limitations of state of the art of hybrid pixels are the large material budget, the large power consumption and the expensive production cost due to the bump-bonding technique.

The aim of the LePix project is therefore to design and implement a novel, fast and radiation hard monolithic detector using standard CMOS processes that combines MAPS and hybrid pixel detectors advantages.
According to the monolithic approach, both the sensor and the read-out electronics are integrated on the same silicon wafer. The LePix key feature is the charge collection by drift, which is expected to improve both speed and radiation hardness. Hence the main challenge is building the sensor and its processing electronics on a single reverse-biased substrate. The implementation of the front-end electronics using standard microelectronics technologies reduces production cost. At the same time high production rates (about 20 m^2/day) become possible.

At present the project involves CERN, INFN (Turin, Padova, Bari and Bologna sections), IReS in Strasbourg, Imperial College and the C4i-MIND foundation. Within this framework, the INFN of Turin has given its contributions both in the front-end design and in first prototypes tests.

Chapter 3

LePix

3.1 Basic sensor layout

A simple sketch of a single pixel cell is shown in Figure 3.1, in which we can recognize the most important features of the LePix detector.
The bulk of the sensor is a p-type substrate, with a n-well collection electrode. The first transistor (input device) of the read-out electronics chain is built into the n-well itself. The key difference with respect to traditional MAPS is the reverse bias voltage applied to the substrate. Hence, the substrate is partially depleted and the charge collection is fully dominated by drift as in hybrid pixel detectors, in order to guarantee adequate speed and radiation hardness.

Although this sensor concept is intuitive on paper, pratical design and implementation of the device structure are challenging.
The parasitic capacitance of the collection electrode, which provides the charge to voltage conversion, must be minimized in order to maximize the convertion gain for a certain fixed signal-to-noise ratio. This is achieved minimizing the pixel area and using *high resistivity* substrates ($> 100\,\Omega\,\mathrm{cm}$).
Note that differently from MAPS, due to the charge collection by drift the collection electrode can be made large enough to host the input transistor. However the space available to put electronics is limited to the collection electrode itself, hence the circuitry integrated on the pixel surface is kept to the bare minimum and it is limited to the input transistor only.
Furthermore, all NMOS transistors in LePix must be insulated from the reverse biased substrate, requiring all NMOS devices in *triple well*. Hence due to the lower occupancy a PMOS input device is preferable in LePix.
The remaining analog and digital circuitry works at the periphery of the sensitive region, but integrated on the same piece of silicon using standard CMOS technologies.

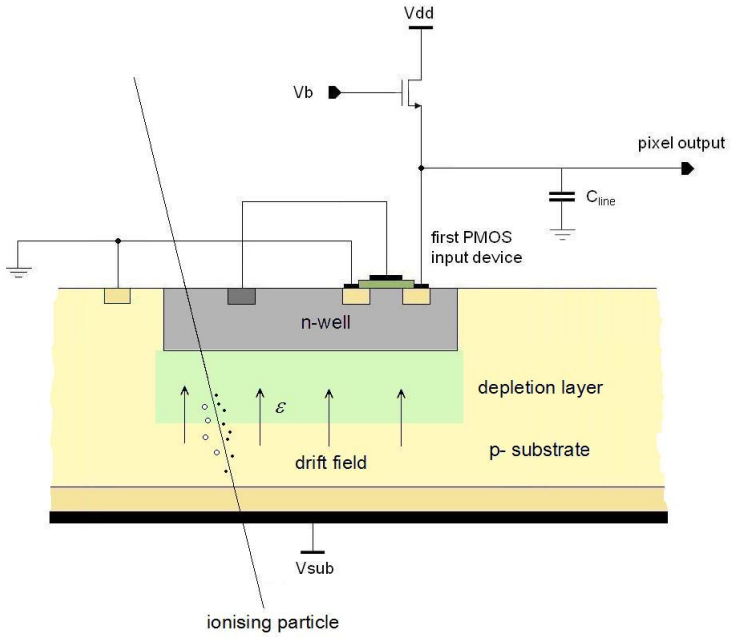

Figure 3.1: LePix: basic sensor concept.

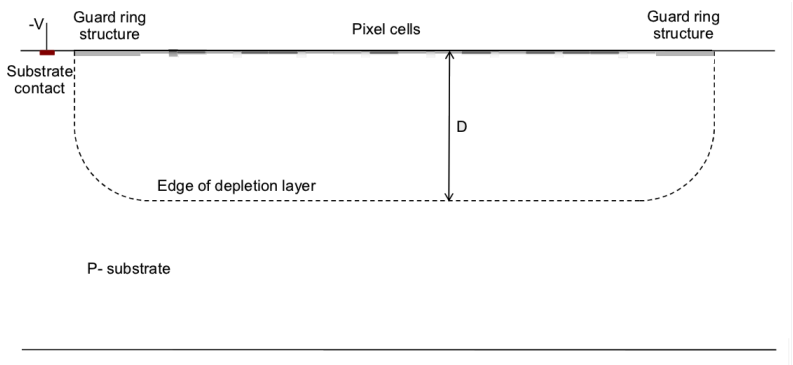

Figure 3.2: External guard ring structure which ensures a uniform depletion layer in the substrate.

This is another key aspect of LePix, which exploits the possibility offered by a few silicon foudries of porting standard CMOS processes on high resistivity wafers. This aspect introduces further challenges. In particular a n-well of low resistivity ($\sim 1 \div 2\ \Omega$ cm) hosts the read-out electronics at the border of the sensitive region. However it forms with the high resistivity p substrate a reverse-biased diode. Hence the n-well must be sufficiently insulated from the substrate in order to avoid breakdown phenomena.
On the other hand a uniform depletion layer is essential for a homogeneous sensor response. As shown in Figure 3.2 this is achieved implementing an external guard ring structure around the pixelated area. Simulations of the sensor have been shown that a uniform depletion layer of $30 \div 40\ \mu$m should be obtained by applying a -100 V reverse bias, with an electric field sufficiently low to avoid breakdown.

In order to comply with the nominal 25 ns LHC bunch crossing, a simultaneous (parallel) read-out of each pixel of the matrix is required. This represents another key difference with respect to standard MAPS, which use serial read-out schemes instead. The drawback is that a parallel read-out requires at least one independent metal line for each pixel, leading to a very high interconnection density and requiring ultra-fine pitch lithography. For this reason project developers choose the standard 90 nm CMOS technology.

3.2 Front-end electronics - general aspects

As mentioned above, the integrated electronics on the pixel is limited to the first transistor only. The output signal can be read-out either at the source or at the drain of the device. Hence two possible schemes for the analog front-end electronics can be explored: a *voltage mode* or a *current mode* read-out.

As shown in Figure 3.3, in the first case the input transistor is in source follower (SF) configuration and works as a voltage buffer. Thus the transistor output signal is sensed at the source. In a realistic front-end chain the source is AC coupled to a voltage amplifier-shaper stage followed by a comparator, which provides a digital output pulse after a particle hit. Furthermore, a measurement of the initial charge can be performed by using the Time over Threshold (ToT) technique applied to the discriminator digital output pulse.

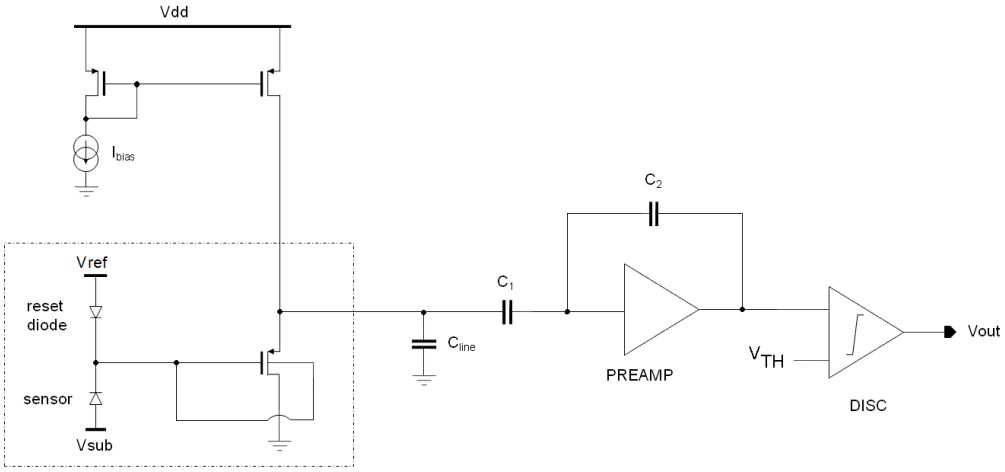

Figure 3.3: Voltage mode read-out.

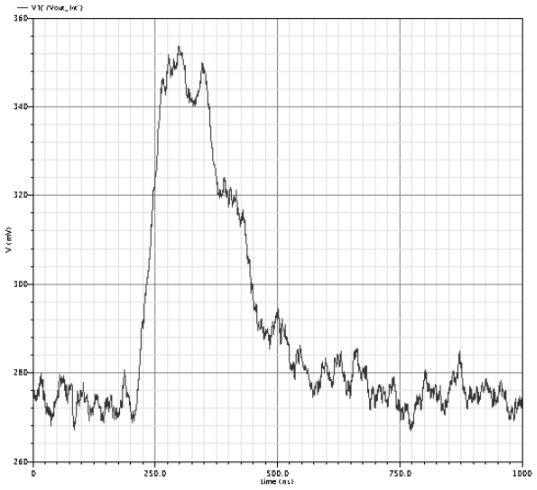

Figure 3.4: Voltage mode CAD simulation. Signal at the voltage amplifier output, obtained from a 1200 electrons signal with an ideal target power consumption of 1 μW/cm^2 and assuming a sensor capacitance of 10 fF with $C_{line} = 2$ pF

In this architecture a single line per pixel is required to bias the input device and to sense the output signal. The voltage mode read-out has therefore the main advantage of stacking only two transistors (the input device and its load) within the V_{DD} voltage supply.
This leads to very low voltage operation and power consumption, ensuring at the same time enough voltage headroom for leakage-induced DC variations. Note that the capacitor C_{line} is not a physical element, but represents the parasitic capacitance of the metal connection. The rise time of the signal (but not its amplitude) is sensitive to this parasitic capacitance.
In Figure 3.4 is shown a simulation of the signal at the voltage amplifier output, obtained from a 1200 electrons charge signal with an ideal target power consumption of 1 μW/cm^2 and assuming a sensor capacitance of 10 fF with C_{line} = 2 pF. In this conditions the simulated equivalent noise charge (ENC) is about 40 electrons, whereas the minimum signal necessary to have a 25 ns response is about 2000 electrons.

The second possibility is a current-mode read-out. As depicted in Figure 3.5 the input transistor, in cascode configuration, converts the gate signal into a current, which is fed to a common gate stage and then presented to a current-mode comparator.
In this architecture two independent lines for each pixel are required, one to set the bias current which flows into the input device, and the other one to sense the drain output current. The main drawback of this read-out scheme is the stack of at least four transistors within the voltage supply. This is possible due to the weak invertion operation, leaving however a little voltage headroom for DC variations with respect to proper bias conditions.
On the other hand, the current-mode allows the realization of a more compact front-end cell. Furthermore, this read-out scheme is preferable exploring the maximum possible chip size (typically 2 cm $\times$ 2 cm), affected by a much larger parasitic capacitance of the line.
It is important to note that both the line capacitance at the source and at the drain of the input device are fundamental in the shaping of the signal, but with two different behaviours. The capacitance at the source is benefical, since it bypasses the output resistance of the bias transistor, which tends to reduce the effective transconductance of the input device. The capacitance at the drain, on the other hand, filters the signal, limiting the output swing available to drive the following stages.

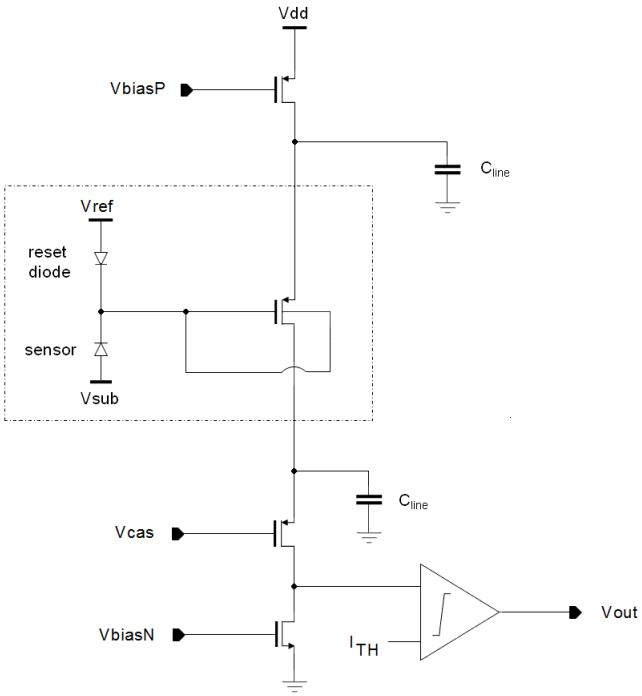

Figure 3.5: Current mode read-out.

3.3 Digital read-out

A parallel signal processing in the LePix architecture becomes a challenge, requiring a sophisticated digital read-out.
In order to process independently the signal of every pixel, at least one metal line for each one is needed, leading to an extremely high interconnection density. This can be reached only with a very submicron CMOS technology as the selected 90 nm. The minimization of the digital power consumption is another critical issue. The analog power is essentially determined by the signal-to-noise ratio required and it is easily predictable once the analog blocks are defined. In contrast, the digital power depends on the switching activity, therefore it can be quite different even for the same architecture working under different occupancy conditions. Hence the digital logic must be minimized. Furthermore, signals are sent in analog form towards the periphery of the matrix, with the clock distributed only in the periphery. Another critical issue is the local data storage, because in order to minimize the power consumption only valid hits must be stored, requiring efficient zero suppression schemes. If the detector has to contribute to the high level trigger primitives also the off-chip data transmission becomes important. Finally, the design of the digital part is complicated by the fact that as already mentioned in LePix all NMOS transistors must be in triple-well in order to insulate them from the reverse-biased substrate. This means that the development of a specific custom digital library is required to perform CAD simulations. The insulation from the substrate high voltage requires also the implementation of novel protection structures against electrostatic discharge (ESD structures).

The target for the digital read-out power consumption is 10 mW/m^2, which summed to the same power budget of the analog read-out gives a total power dissipation of 20 mW/m^2 in continuous operation.

Chapter 4

The first 90 nm LePix submission

4.1 Prototyping strategy

In this chapter a detailed description of the first March 2010 LePix submission in 90 nm CMOS technology is given.
Breakdown and transistor test structures, a large diode for radiation tolerance measurements and 4 test pixel matrices have been submitted with the foundry on *standard resistivity* wafers. According to measurements and results presented in this work our desription is only focused on matrices, in which detecting elements and read-out electronics have been integrated on the same piece of silicon.

Actually, a prototype of the LePix digital circuitry has not yet been implemented. Thus matrices have been instrumented with some few simplified read-out schemes.
Two matrices use an analog serial read-out based on source followers, similar to traditional MAPS. The other two matrices are equipped with the analog front-end expecially developed for the LePix project, implementing the previously described voltage-mode read-out followed by a binary serial read-out. No support for ToT is available. A second submission on *high resistivity* substrates (spring 2012) will contain more complete front-end electronics, including first prototypes of the digital circuitry.

At first the general segmentation of the matrices is discussed. Then a detailed description of the front-end electronics schemes is given.

4.2 Pixel matrices segmentation

All matrices exhibit the same basic structure. As shown in Figure 4.1 the sensitive area, the analog read-out and a bare minimum digital circuitry have been implemented on the same chip (2 mm $\times$ 2.5 mm) inside a special guard ring structure (about 200 μm around the matrix).
Analog and digital power are separated, with a nominal voltage supply V_{DD} = 1.2 V for both. The substrate can be depleted by applying a reverse bias on the dedicated pad outside the guard.
The pixel segmentation is the same for all matrices. Each chip contains in total 1216 pixels divided into 38 rows $\times$ 32 columns. Furthermore, the sensitive area is divided into two asymmetric regions. An upper part, referred to as TOP part, and a lower part, referred to as CORE part.
The TOP part contains 192 pixels in 6 rows $\times$ 32 columns, whereas the CORE part 1024 pixels in 32 rows $\times$ 32 columns. All matrices have the same TOP part read-out electronics, but differ in the CORE part one.
In order to avoid confusion, from now we refer to matrices as M1, M2, M3 and M4.

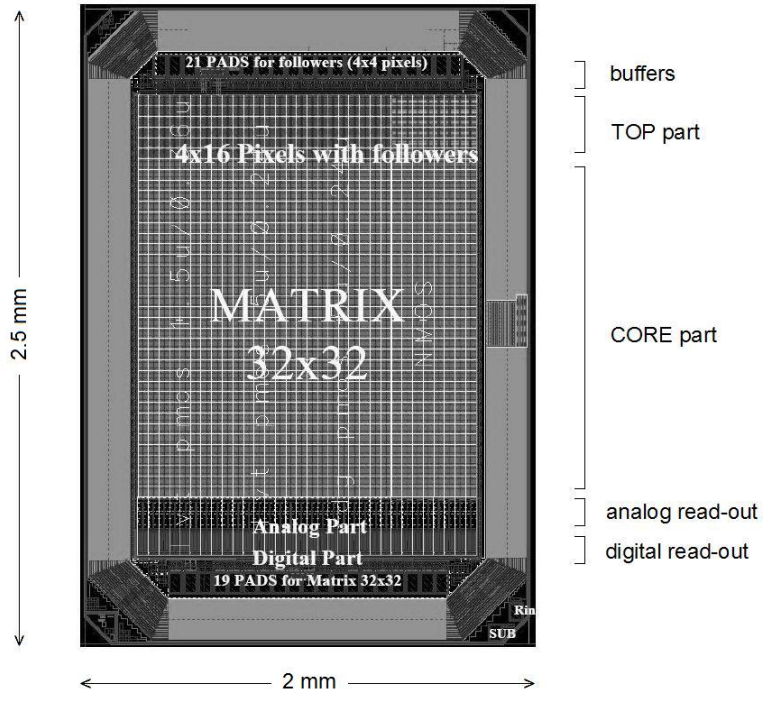

Figure 4.1: Overall layout of matrices.

Output voltages of the TOP part pixels are connected to analog buffers in order to allow a direct access with a probe.
On the other hand, CORE part pixels of matrices M1 and M2 are equipped with a MAPS-like *analog* serial read-out based on source followers, whereas matrices M3 and M4 implement a simplified preamplifier-comparator front-end chain with a *binary* serial read-out.

All pixels in all 4 matrices have a PMOS or a NMOS input transistor in source follower configuration as first device of the read-out chain, built on the collection diode itself. In particular, 4 different types of input transistor have been implemented, using two sizes of thin oxide PMOS, a thick oxide PMOS and a NMOS in order to explore different sensor optimizations. Hence in each matrix we can recognize a vertical segmentation into 4 macro-columns with 8 columns each one. Pixels of each macro-column have the same input transistor, as depicted in Figure 4.2.
Thin oxide PMOS input devices exhibit more gate leakage, whereas this issue does not affect thick oxide PMOS. Furthermore, in PMOS devices the source-bulk junction is slightly forward biased. NMOS input transistor instead have a much larger parasitic capacitance in the pixel, because implemented as triple-well NMOS. As mentioned in Chapter 3, a PMOS input device is preferable in LePix due to the low area of the pixel cell.

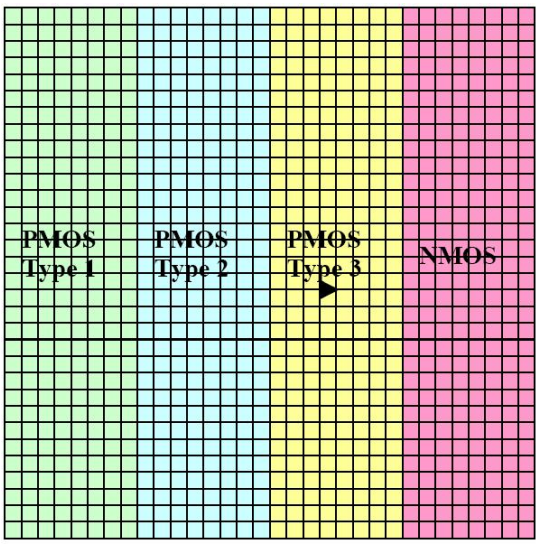

Figure 4.2: Vertical matrix segmentation. In order to explore different sensor optimizations 4 types of input transistor have been implemented.

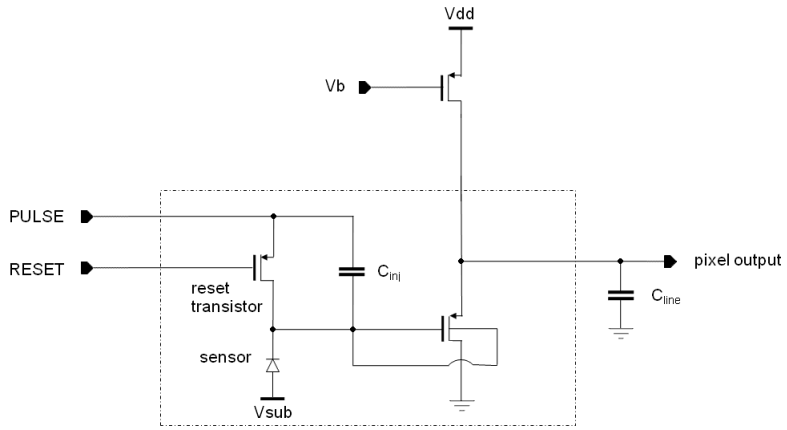

Figure 4.3: Avtive-reset pixel cell.

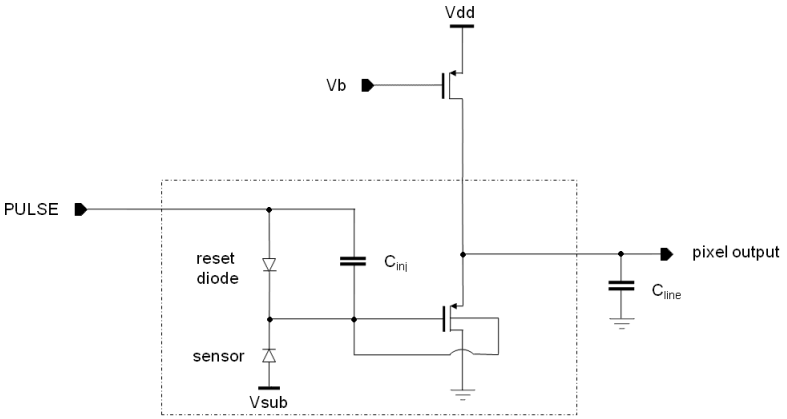

Figure 4.4: Continuous-reset pixel cell.

In matrices M1 and M3 the collection electrode size has been kept very small (3.75 μm $\times$ 3.75 μm) in order to minimize the sensor capacitance, whereas it is larger (8 μm $\times$ 8 μm) in matrices M2 and M4. Reducing the collection electrode tends to increase the drift field, hence matrix M1 and M2 represent a more aggressive approach, M2 and M4 a more conservative one.

Each sensor needs to discharge the sensor capacitance after a particle has been detected. Two discharge schemes have been implemented, *active-reset* and *continuous-reset*, sketched in Figure 4.3 and 4.4 respectively.
In active-reset pixels, a PMOS reset transistor is employed to reset the sensor. The PMOS source is kept to a certain reference DC voltage and a CMOS digital voltage pulse PIX_RESET is applied on the gate. Hence a weak-inversion current discharges the pixel capacitance after that some signal charge has been collected. Depending on the duration of the PIX_RESET signal, the reset transistor can behave like a switch or like a linear resistor. On the other hand, continuous-reset pixels discharge the sensor capacitance through a diode connected to the reference DC voltage which absorbs the leakage current from the pixel.
In each matrix all pixels of the TOP part implement the active-reset scheme. In the CORE part 16 rows use the active-reset and the remaining 16 rows the continuous-reset, as depicted in Figure 4.5.

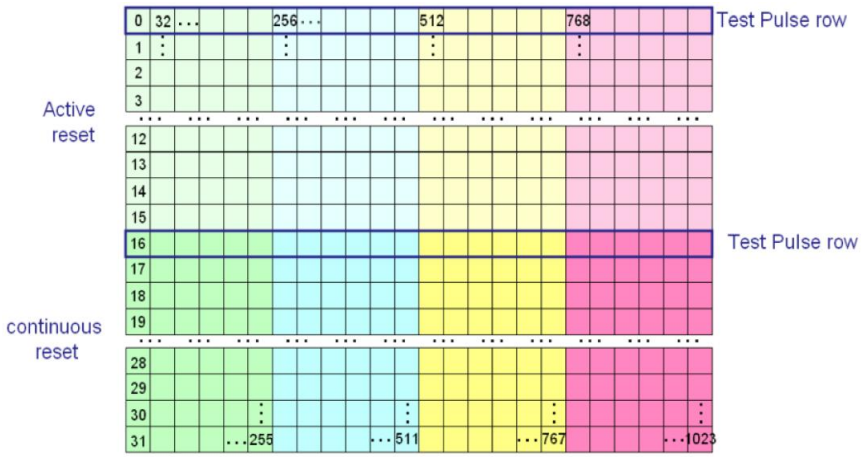

Figure 4.5: CORE part segmentation.

Three rows in each matrix can be electrically pulsed by applying a voltage step V_{PULSE} (test pulse) over a injection capacitor C_{inj} (1 fF from specifications). This allows the characterization of the sensor and of the read-out electronics. Also in the other rows the injection capacitor is implemented, but it is connected to the fixed reference DC voltage.
In particular, in the TOP part the lower row can be electrically pulsed. In the CORE part instead, the PULSE signal can be applied to the first active-reset row (row 0) and to the first continuous-reset one (row 16), in order to avoid a large perturbation of the matrix. Therefore only 32+32 pixels receive the pulse in the CORE part and 32 pixels in the TOP part. The test pulse is applied at the same time to all pulsed rows.

4.3 Matrices TOP part read-out

The matrix TOP part (6 rows $\times$ 32 columns, all active-reset input devices) is the same for all 4 matrices.
As depicted in Figure 4.6, following the vertical segmentation in macro-columns the TOP part is split in 4 sub-groups of 6 rows $\times$ 8 columns each one, corresponding to 4 different input devices. However only 16 pixels for each sub-group can be electrically connected to the output through analog buffers. The remaining pixels located aroud them ensure a uniform depletion layer under each 4 $\times$ 4 center region. An external multiplexer (MUX) allows to select which sub-group must be electrically connected to the output, using two CMOS digital signals SELECT_1 and SELECT_2 (i.e. 00 connects the first thin oxide PMOS sub-group, 01 the second one, 10 the thick oxide PMOS sub-group and finally 11 the NMOS last one).
Furthermore, pixels of the last row can be electrically pulsed, hence a complete characterization and calibration of the TOP part analog read-out chain can be performed.

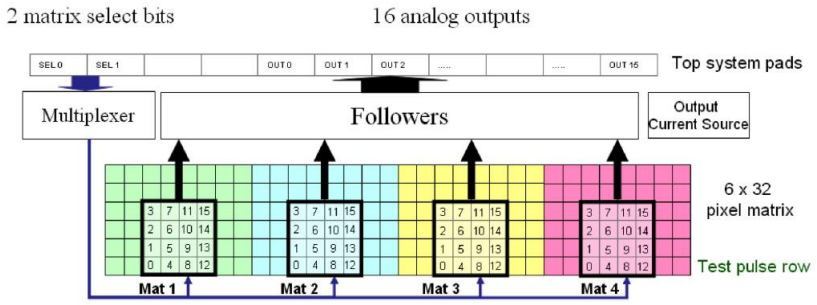

Figure 4.6: TOP part architecture.

The analog-buffers block contains 4 different sub-blocks, one for each 4×4 sub-group. Then each sub-block consists of 16 building blocks, one for each pixel.
As sketched in Figure 4.7 for a PMOS active-reset cell, the read-out electronics at the periphery of the TOP part is extremelly simple and involves only a CMOS switch and a NMOS transistor in source follower configuration biased with a NMOS current mirror. The electronics integrated in the pixel cell is limited to the input device only in source follower configuration, with a injection capacitor and a PMOS reset transistor. The input device is biased with a PMOS load built at the periphery. The switch is used to select which sub-matrix needs to be biased, because the current mirror is in common between the multiplexed pixels, whereas there is a NMOS source follower for each pixel.

As shown in the simplified schematic in Figure 4.8, the input transistor and the NMOS one in source follower configurations work as voltage buffers. Therefore the main advantage of these read-out scheme is the possibility of probing the pixel output signal directly with an oscilloscope.
In order to reduce the deep triode on-resistance the CMOS switch connected between the NMOS source follower and the current mirror load is implemented using wide devices (remind that $R_{on} = \left[\, \mu C_{ox} \frac{w}{L} (V_{GS} - V_{TH}) \,\right]^{-1}$).
The capacitor C_{line} in the schematic is not a physical element, but represents the parasitic capacitance of the metal line (estimated 28 fF). Whereas C_{bus} represents the total output capacitance, i.e. the total capacitance of the output pad including the probe parasitic capacitance (3 pF in simulations).
The NMOS bias current can be set using the IBIAS pin and has a nominal value of 50 μA.

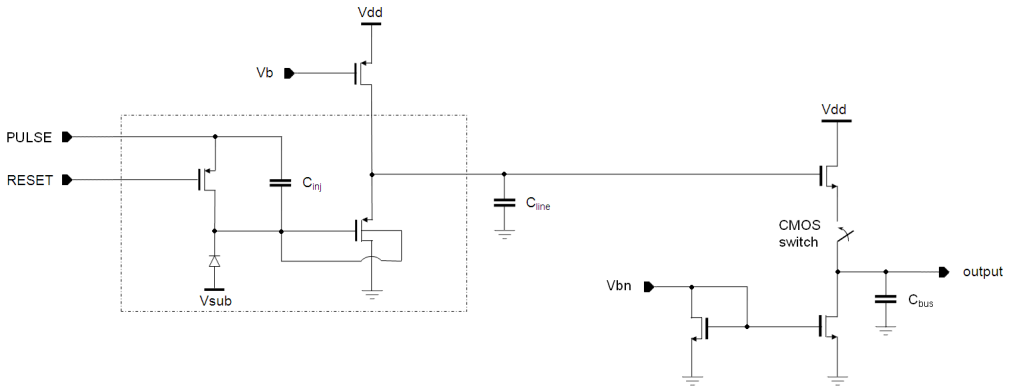

Figure 4.7: Schematic of the TOP part read-out.

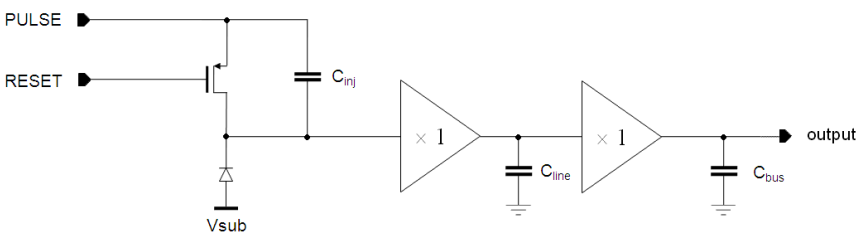

Figure 4.8: TOP part simplified schematic.

4.4 Matrices 1-2 CORE part read-out

In order to optimize the sensor characterization, the CORE part of matrices M1 and M2 has been equipped with a simple analog serial read-out based on a *double voltage sampling* with source followers.
For each pixel two analog voltages V_{MEM1} and V_{MEM2} are sampled and stored, the first after a digital pulse MEM1, the second one after a tunable time using another digital pulse MEM2. The difference between these two stored voltages corresponds to the signal collecteted by the pixel added to the integrated pixel leakage current.

The circuit is shown in Figure 4.9 for an active-reset pixel cell.

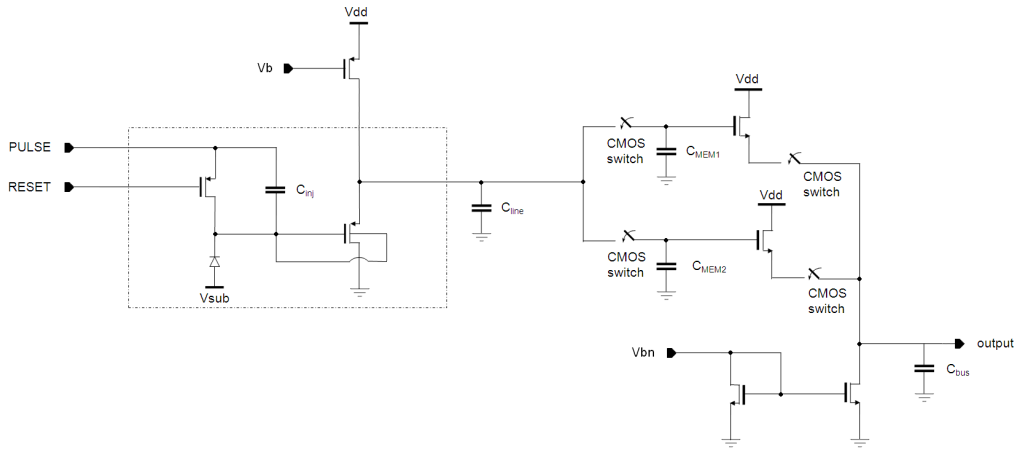

Figure 4.9: Matrix 1-2 analog read-out.

The electronics integrated on the sensor is the same described for the TOP part, with a PMOS (or NMOS) source follower input device, the injection capacitor C_{inj} and the PMOS reset transistor (or a diode in continuous-reset pixels). At the periphery instead, a first couple of CMOS switches driven by MEM1 and MEM2 digital pulses is used to sample the pixel output voltage on two storage capacitors C_{MEM1} and C_{MEM2}. Each switch is implemented with a couple of regular PMOS and NMOS small transistors, in order to reduce as possible the leakage current through C_{MEM1} and C_{MEM2}. The storage capacitors are implemented as wide metal-to-metal structures, with a nominal capacitance of (270 $\pm$ 2) fF. The capacitor C_{line} represents the parasitic capacitance of the metal line from the pixel to the periphery of the matrix, extimated to be (200 $\pm$ 2) fF.

After this stage, two NMOS in source follower configuration work as voltage buffers, one per storage capacitor. They transfer the analog voltages stored in the C_{MEM1} and C_{MEM2} capacitors to the output pad with an almost unitary gain. Furthermore, the source follower configuration ensures proper impedance matching. A second couple of switches, driven by digital signals generated by the digital circuitry, is used to select the storage capacitor during the read-out phase. Hence the current flows only through the selected transistor, minimizing the power consumption. The bias current is generated with a NMOS current mirror controlled by an external bias resistor and can be adjusted between 50 μA to 400 μA.

The digital circuitry is very minimal and involves a serial read-out based on 2048 D-Flip/Flops (DFF) configured as a shift register, two devices for each pixel, as depicted in Figure 4.10.

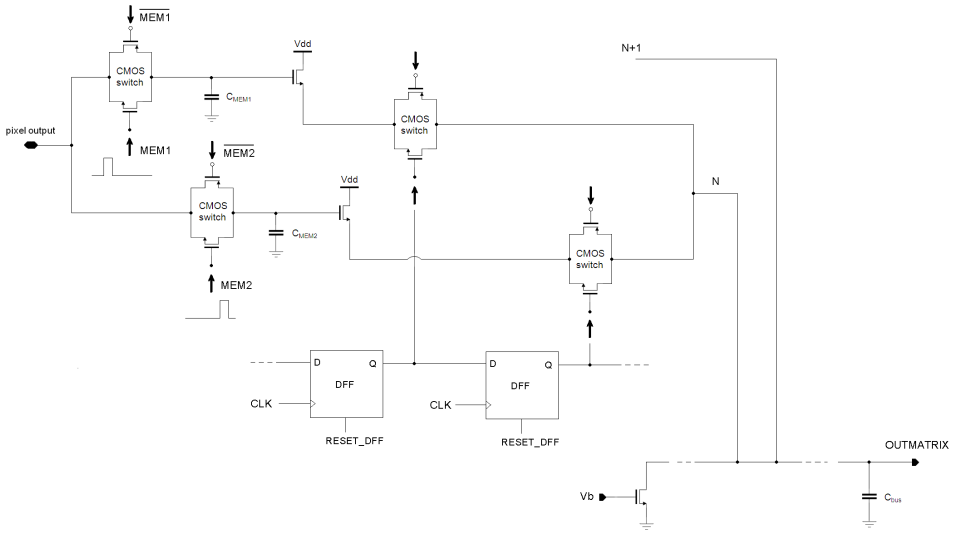

Figure 4.10: Matrix 1-2 digital part.

The acquisition and read-out procedures are controlled by 5 external CMOS digital signals: START, RESET_DFF, MEM1, MEM2 and CLOCK. The signal timing is sketched in Figure 4.11.
During the *acquisition time* START is high, while during the *read-out time* START is low. When START is high the CLOCK is not propagated and flip-flops are resetted by RESET_DFF (at least 1 μs). Each DFF output is 0 therefore output switches are open. The two sampled voltages V_{MEM1} and V_{MEM2} are stored when MEM1 and MEM2 digital signals drive the first couple of CMOS switches.

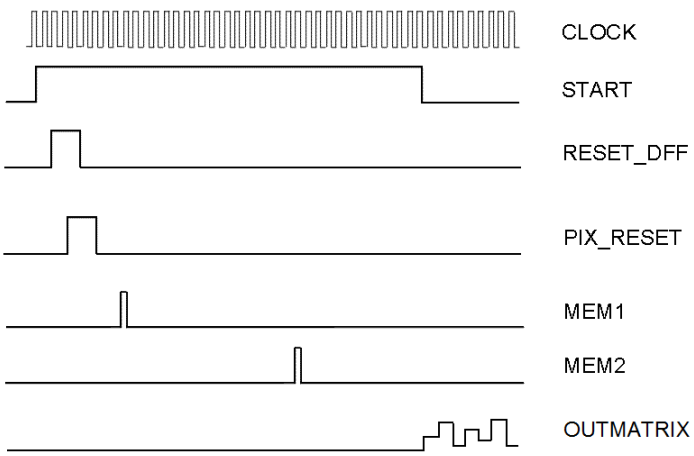

Figure 4.11: Matrix 1-2 signal timing. The CLOCK is propagated in DFFs only when the START is low, allowing the serial read-out of all 1024 pixels in the CORE part.

The time interval between MEM1 and MEM2 defines the actual acquisition time, evaluated between the MEM1 falling edge and the MEM2 rising edge. When START flips to zero the CLOCK is propagated to DFFs and the input of the first DFF is set to 1. Thus, being the DFF a *clocked* device, the input is shifted in output only when a clock rising edge occurs. Hence with the first clock cylcle this 1 closes the C_{MEM1} output switch, the next clock cycle the 1 shifts to the second DFF output and the C_{MEM2} ouput switch is closed, providing two stored voltages for the first pixel. The same procedure occurs for all other pixels, implementing a serial read-out of the CORE part.
Two clock cycles are required for each pixel, therefore 2048 clock cycles to read-out the entire CORE part (e.g. 2.48 ms with a 100 kHz CLOCK frequency).
The output pad OUTMATRIX is unique, thus the output signal is a sequence of 2048 *analog* voltages V_{MEM1} and V_{MEM2}, two stored values for each pixel. After 2048 clock cycles the read-out procedure is performed again, unless START returns high.

This read-out scheme is very similar to standard MAPS, although here the two voltages are stored outside of the pixel, because the electronics is built at the periphery.

4.5 Matrices 3-4 CORE part read-out

A more realistic and robust analog front-end scheme (expecially designed for the project) has been implemented in matrices M3 and M4 CORE parts. A schematic of the analog part is shown in Figure 4.12.
Every pixel is equipped with a *binary* serial read-out with the input transistor in source follower configuration AC coupled to a voltage amplifier (PREAMP) followed by a comparator (DISC). This is a classical (but in very deep submicron technology) front-end scheme, which explores the voltage-mode read-out described in Chapter 3.
The output provided by the DISC is a CMOS 1.2 V logic signal. If the DISC input signal is below a certain threshold DC level V_{TH} the output is zero. In contrast, when the input exceeds the threshold the ouput flips to the voltage supply V_{DD}, corresponding to 1.
Hence if a particle hit is sensed, the DISC produces a digital output pulse, which can be stored by a flip-flop. With a more sofisticated circuitry, ToT can be also implemented, allowing a measurement of the charge induced in the sensor by a ionizing particle.

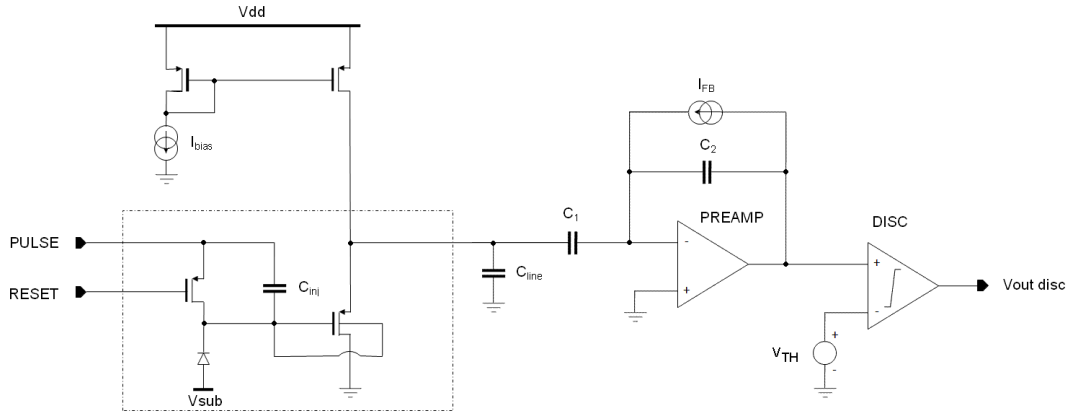

Figure 4.12: Matrix 3-4 analog read-out.

Detailed schemes of PREAMP and DISC will be described (at the transistor level) in Chapter 5, describing devices bias characteristics.

The digital read-out scheme is shown instead in Figure 4.13. Similar to matrices M1 and M2, the acquisition procedure is *serial* and is controlled by 3 external CMOS digital signals: START, RESET_DFF and CLOCK. The architecture is based on a shift register consisting of 1024 D-Flip/Flops (DFFs), one device for each pixel.
In particular, the digital circuitry involves two multiplexers (MUX) and a DFF for each pixel. The first MUX feeds the DISC output signal and the CLOCK, while its output is fed to the DFF clock input. The second MUX has one input which feeds the N-1th pixel digital output, whereas the other one is permanentely set to 1. The START drives the multiplexers switch activity and RESET_DFF resets the DFF.

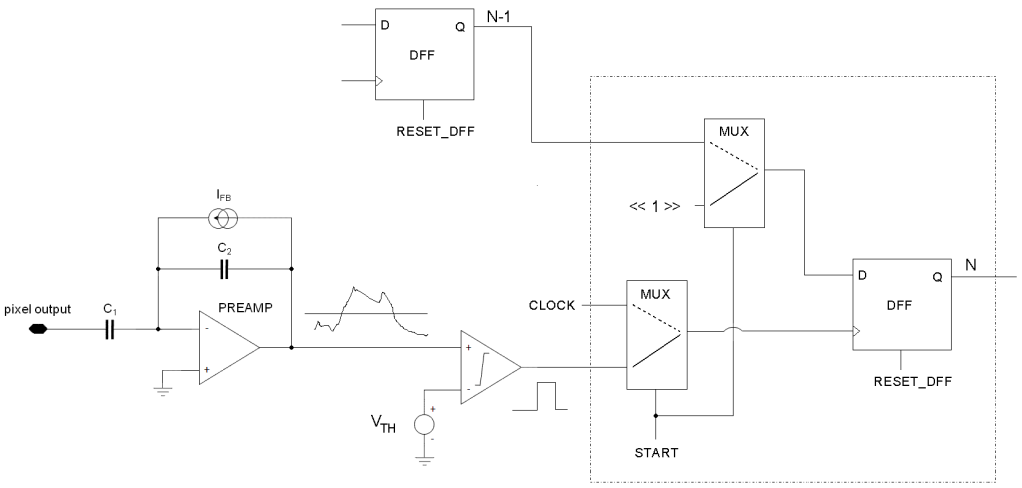

Figure 4.13: Matrix 3-4 digital part.

The signal timing is shown in Figure 4.14. Similar to matrices M1 and M2, there are an *acquisition time* when START is high and a *read-out time* when it is low.
During the first phase, the DFF is resetted by RESET_DFF, hence its output is 0. At the same time the DISC output can be propagated to the DFF clock input. Therefore if the sensor registers a particle hit (or any other transition occurs in the DISC, due to some noise for example) the DISC digital pulse works as a clock cycle for the DFF (remind that a DFF is a *clocked* flip-flop) and the bit 1 from the second MUX is propagated in output. Otherwise, if no digital pulse is produced by the DISC the DFF output remains to 0.

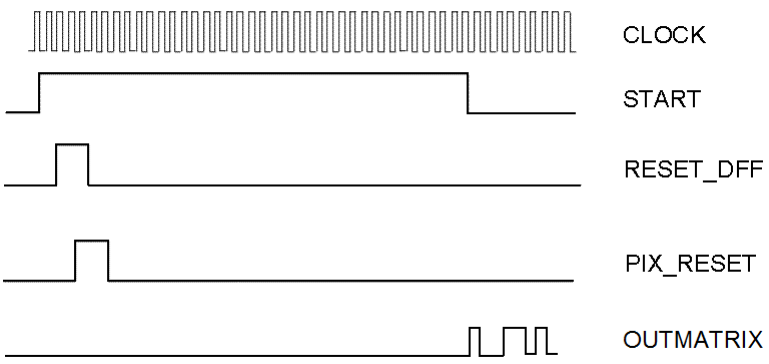

Figure 4.14: Matrix 3-4 signal timing.

On the other hand, when START is low multiplexers inputs switch to the external CLOCK and to the N-1th DFF output respectively. Hence, with this architecture the DFFs are configurated as a shift register and a serial read-out of all 1024 stored bits is performed, requiring 1024 clock cycles to read the entire CORE part.

We stress that differently from the matrix M1 and M2 serial read-out, in which the output is an array of 2048 *analog* voltages (i.e. V_{MEM1} and V_{MEM2}), in this case the output is a simple array of 1024 *digital* CMOS voltages.
Being sensitive to sudden signals only and providing a binary output, this front-end scheme can be exploited in a first *test beam*, in order to explore LePix capabilities.
Prototypes with a further *filtering* stage (shaper) are also planned, in order to filter the PREAMP signal.

Chapter 5

Experimental setup and measurements

5.1 Experimental setup in Turin

Within the LePix collaboration, INFN has been an important reference point, providing the design of the matrices 3-4 analog read-out (Turin) and the test-bench to perform characterizations (Padova).

The experimental setup is shown in Figure 5.1 and includes a main test PCB, some standard power supplies, a waveform generator, a digital oscilloscope and a specific DAQ system. The test-bench is installed in the INFN laboratory in Turin since April 2011.
The chip is wire-bonded onto a mezzanine which provides mechanical support and output test points. The mezzanine is equipped with a bare minimum standard circuitry. In particular the matrix output is fed to an operational amplifier (OPAMP) followed by a fully differential amplifier (FDA). The mezzanine should also host the integrated circuits which control switches of the TOP part analog read-out with buffers, but at present the firmware for these devices is not available. Hence they have not been mounted and only NMOS transistors can be observed at the oscilloscope.
As shown in Figure 5.2, the mezzanine is then plugged onto the test PCB, equipped with some trimmers and further output test points. Both the mezzanine and the test PCB have been provided by the INFN of Padova.

At the time of writing a matrix M1 and a matrix M3 have been wire-bonded onto two different mezzanines, requiring each one some different specific electrical connections and discrete components.

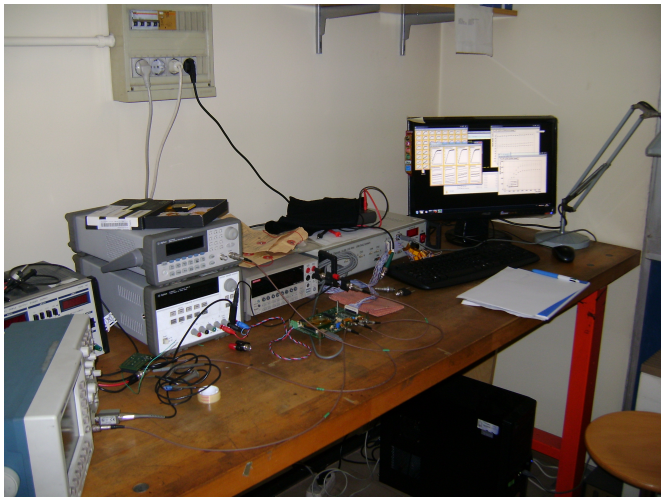

Figure 5.1: Experimental setup in Turin.

A standard power supply is employed to bias the test PCB with a nominal value of 5 V.
Another power supply is required to suppress with a reverse bias of -12 V the parasitic transistors which are introduced to comply with the pattern density rules of the foundry. A third power supply provides the reverse bias for the sensor substrate.
Moreover, a standard waveform-generator provides the PULSE signal for test-pulse rows.

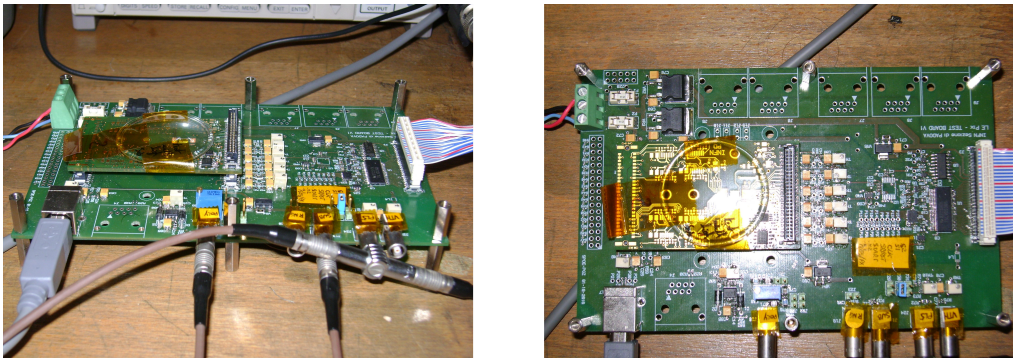

Figure 5.2: Test PCB (INFN of Padova).

Figure 5.3: Data Aquisition (DAQ) system (INFN of Padova).

The test PCB is connected using a standard USB cable to the DAQ system depicted in Figure 5.3, equipped with a Field Programmable Gate Array (FPGA) and a 14-bit ADC. Finally, the DAQ is connected via USB cable again to a PC, equipped with a specific acquisition software interface.

5.2 Acquisition software

At this point a detailed description of the LePix acquisition software is essential in order to understand how all tests and measurements have been performed.
As shown in Figure 5.4, the FPGA inside the DAQ is in communication with a user-friedly software interface, built with ROOT 5.26 [9] and Visual C++ 2010 under Windows 7.

As shown in Figure 5.5 the software is used to set the CLOCK frequency and the timing for digital signals START, RESET_DFF, PIX_RESET (common to all matrices) and MEM1/MEM2 (only for matrices M1 and M2) described in Chapter 4. At present the PULSE width option is not yet implemented.
The software is indispensable for all measurements. The output sequence from the CORE part of each matrix at the end of the read-out chain is fed to a 14 bit ADC and converted into an array of integers, each one between 0 and $2^{14} - 1$. The interface provides the on-line reconstruction of the pixel-map for the matrix CORE part. In particular, selecting the *Soft continuous* acquisition mode the interface provides an on-line monitoring of the matrix. With the *Soft single shot* option instead, a set of data can be stored for subsequent off-line analysis. The software can be used both for matrices M1-M2 (2048 output values) and for matrices M3-M4 (1024 output values) architectures.

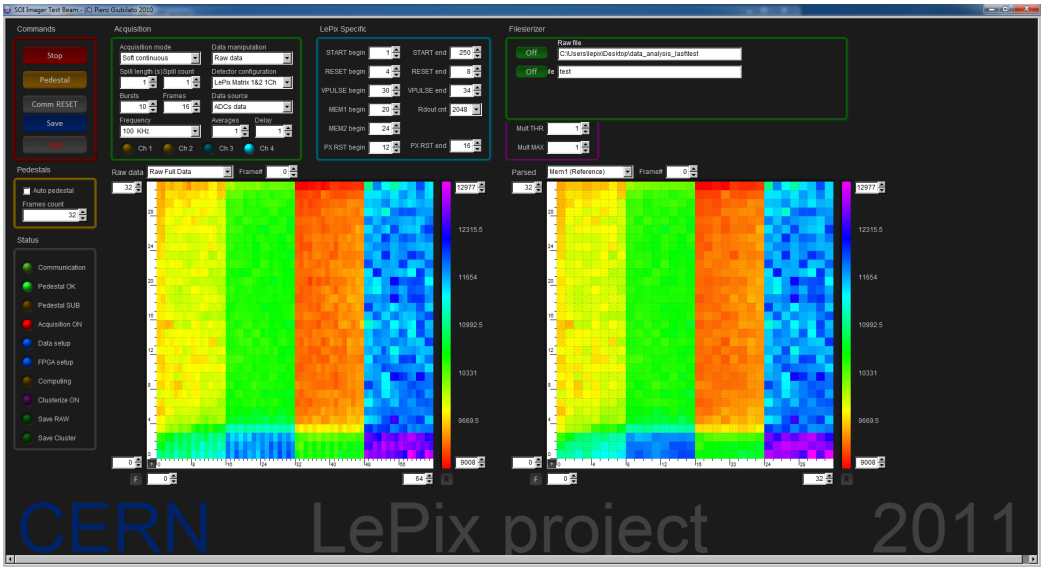

Figure 5.4: LePix software: acquisition interface.

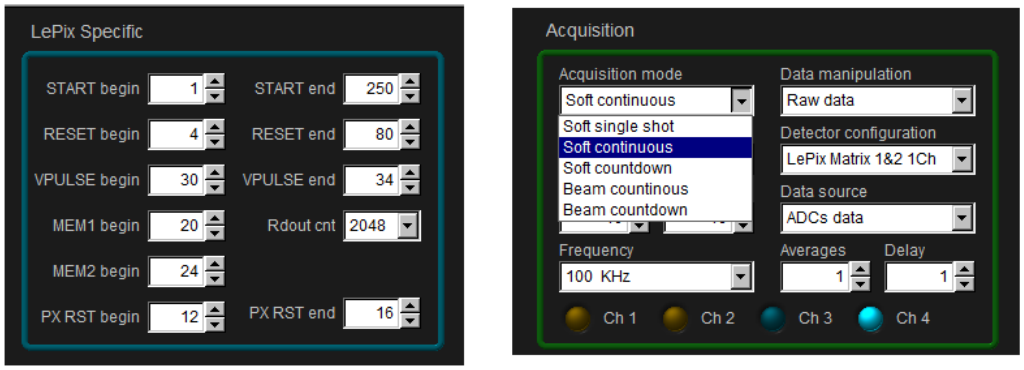

Figure 5.5: Signal timing and acquisition mode settings.

In particular, each *Soft single shot* acquisition produces 3 binary output files of 8 kB each one, ending with SHOT.bin, PED.bin and NOISE.bin. Each file, opportunely converted into a ASCII file with a ROOT macro or a standard C/C++ program, contains a sequence of 2048 integers values, according to its dimension (i.e. 32 bit = 4B for each integer, 1024 pixels in the CORE part, 2048 values stored for each acquisition).

The SHOT file contains values obtained with a *single* acquisition. The PED one, instead, contains values evaluated as an *average* over more consecutive acquisitions (32 by default). In this case the NOISE file contains the RMSs of the PED mean values.
Of course, the meaning of these 2048 integers for matrices M1-M2 is different with respect to matrices M3-M4. In fact, as previously described the serial readout of the CORE part in matrices M1 and M2 produces a sequence of 2048 *analog* voltages V_{MEM1} and V_{MEM2}, two stored values for each pixel. Matrices M3 and M4 have been equipped instead with a *binary* serial readout, and the output produces a sequence of 1024 simple CMOS *logic* values, i.e. a sequence of 0/1. The interface in this case reads 32 DFFs outputs of the first column, forcing the following 32 values to a default, and so on for all 32 columns.
We have to note that actually the acquisition performed for matrices M1-M2 is independent with respect to the chip. In particular, any signal or DC voltage applied to the mezzanine OUTMATRIX pad can be sampled for 2048 clock cycles after the end of START and then reconstructed off-line. For instance, this possibility has been exploited in order to obtain DC and gain characteristics for the external-chip read-out, without a chip wire-bonded onto the mezzanine.

5.3 Measurements and data analysis strategy

All characteristics and measurements have been extracted from SHOT and PED files. In this section a brief description of the overall off-line data analysis strategy is discussed.

As a matter of fact, there was no software for the off-line data analysis, hence the main contribution of the author during his work has been the development of a set of ROOT macros (inside a Windows environment) in order to perform more systematic and faster analysis starting from the binary raw data.
In particular, a first tool is required in order to convert entire folders of binary files into ASCII files, extracting matrices output voltages from ADC integers and pulsed rows values. Moreover, as shown in Figure 5.6 another tool which provides the reconstruction of the serial output and of pixel maps has been developed.

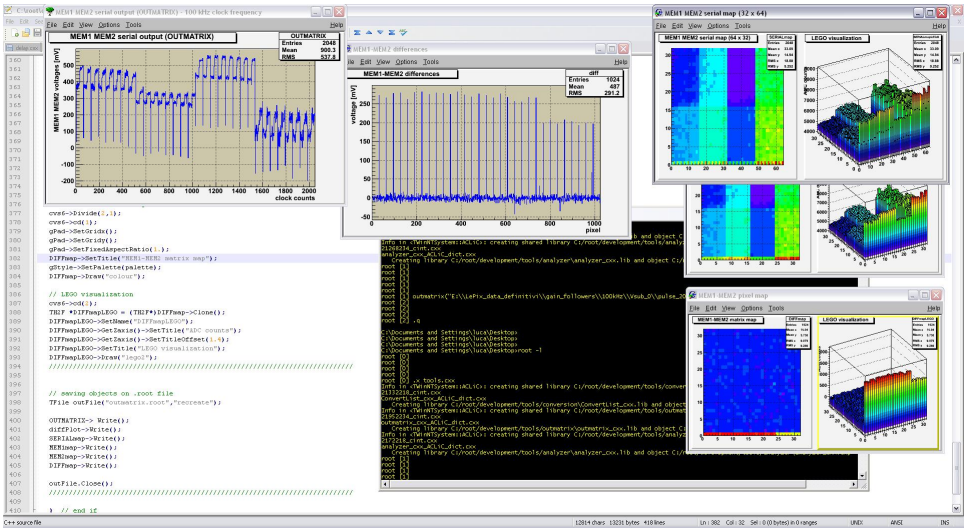

Figure 5.6: Off-line matrix serial output and pixel-map reconstruction.

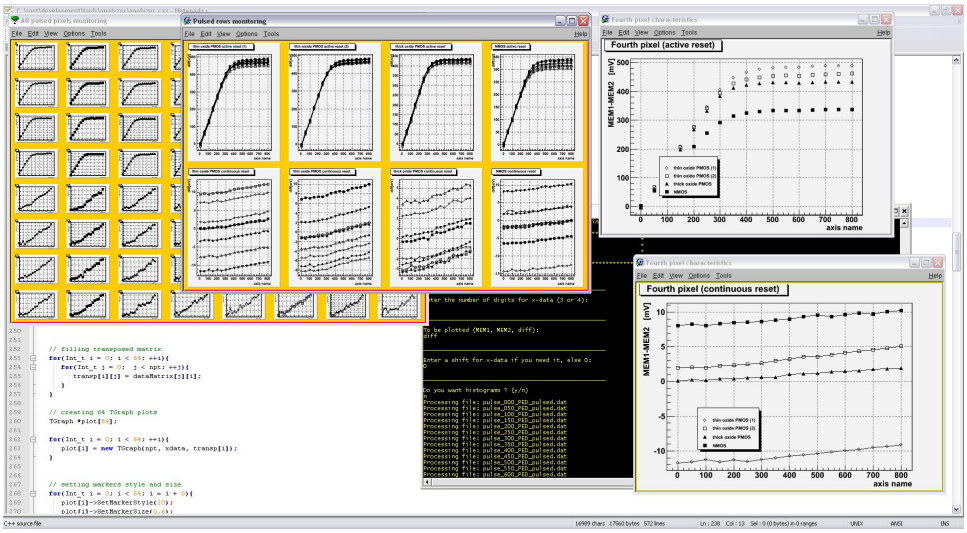

Figure 5.7: Off-line extraction of pixel characteristics.

Furthermore, all characteristics have been obtained by varying a certain parameter (e.g. the PULSE amplitude, the delay between MEM1 and MEM2, the threshold voltage V_{TH}) and collecting a sequence of acquisitions. Hence as shown in Figure 5.7 a third tool which plots output voltages as a function of the parameter under consideration has been implemented, extracting one characteristic for each pixel in the CORE part or for pulsed-rows only.

A layout problem affects all matrices of the first LePix submission and it will be discussed in the next section in more detail.
Due to this issue all measurements and tests have been performed only on the read-out electronics chain, excluding pixels. Although this represents a dramatic limitation, we have to note that the first tests at CERN with breakdown structures and diodes have been mainly devoted to the radiation tolerance and to the measurement of the breakdown voltage. However, a systematic characterization of the read-out electronics embedded in the sensors has not been performed.

The second part of this work gives therefore a detailed description of all measurements and characteristics involving the read-out electronics, which can be summarized as follows:

- setup characterization
  - setup linearity
  - setup noise
- matrix 1-2 CORE part characterization
  - matrix output
  - source followers (SFs) characterizations
  - estimation of the pixel capacitance
- matrix 3-4 CORE part characterization
  - matrix output
  - threshold scan and noise
  - PREAMPs and DISCs homogeneity
  - bias characteristics

Actually, only a matrix M1 and a matrix M3 have been tested, wire-bonded onto two different mezzanines. Thereby a direct comparison between M1 vs. M2 and M3 vs. M4 is not available.

5.4 Short in the guard

Without doubts, the most critical issue in the first submission test structures is the presence of a systematic *short*, discovered during first tests performed at CERN in summer 2010.
As a matter of fact, the design of the LePix layout has been a challenge. On the one hand, specific foundry *pattern density rules* in very deep submicron technologies are very restrictive. On the other hand, several special masks were needed to be drawn, in order to better insulate the electronics from the reverse biased substrate.
Thus, beside the standard masks provided by the foundry, further non standard and *custom* masks have been required by LePix.
Unfortunately, due to a mismatch with the foundry one of these custom masks has been misintepreted and all matrices of the first submission received a systematic p^+ implant in the external guard ring. As depicted in Figure 5.8 (right) it is connected to the voltage supply n^+ implant in the electronics n-well.

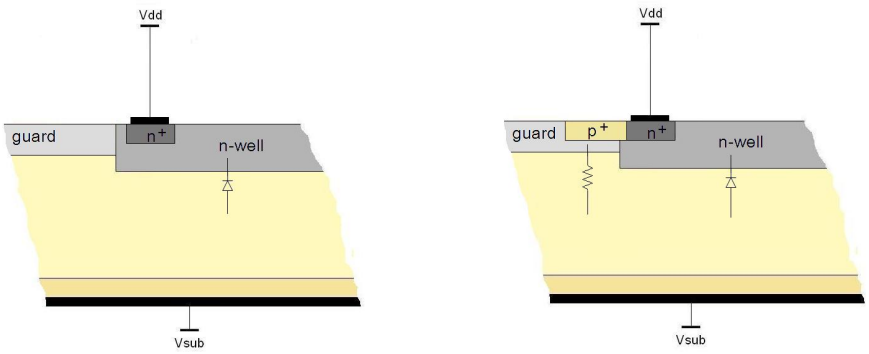

Figure 5.8: Systematic p^+ implant causes a short.

The presence of this short has been found immediately performing first breakdown tests on matrices. The n-well which hosts the read-out electronics and the reverse biased p-type substrate form a reverse biased diode. Hence a measurement of the breakdown voltage is essential, in order to put an upper limit for V_{SUB}.
However, as shown in Figure 5.9, the measurement of the current as a function of the reverse bias exhibits a *linear* trend, in contrast to the expected exponential characteristic of a diode.

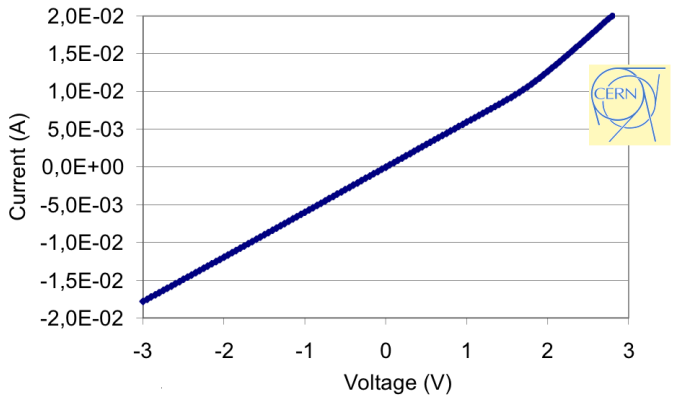

Figure 5.9: Linear behaviour discovered with first breakdown measurements on matrices.

Hence the p^+ implant introduces a *resistive path* of about 80 Ω between the voltage supply V_{DD} and the reverse bias of the substrate, as depicted in Figure 5.10 for an active-reset cell.

A similar p^+ issue has been found in breakdown test structures too, leading to the discovery of the above-mentioned layout problem. However, as shown in Figure 5.11 in this case the measured current follows the right exponential characteristic of a diode. In fact, in the breakdown structure the front-end electronics and hence the shorted n-well are not present.
Therefore breakdown structures do not exhibit the above-mentioned resistive behaviour. A breakdown voltage higher than 30 V (in modulus) has been measured, close to the expected value for these standard resistivity substrates.

Fortunately, only structures on *standard resistivity* silicon wafers received this systematic p^+ implant. The lot on high resistivity substrates was immediately stopped and put on hold after the short evidence, implementing the required corrections.

This short introduces a dramatic constraint, because the nominal reverse biases are forbidden. Hence the chip substrate can not be depleted. If nominal reverse biases are applied, then mA currents flow through the resistive path, whereas typical substrate leakage currents involve a few tens of nA. Under these conditions the chip breaks.
First tests at CERN have been shown that a - 5 V reverse bias is enough to damage the chip, really far from the measured - 30 V breakdown voltage.

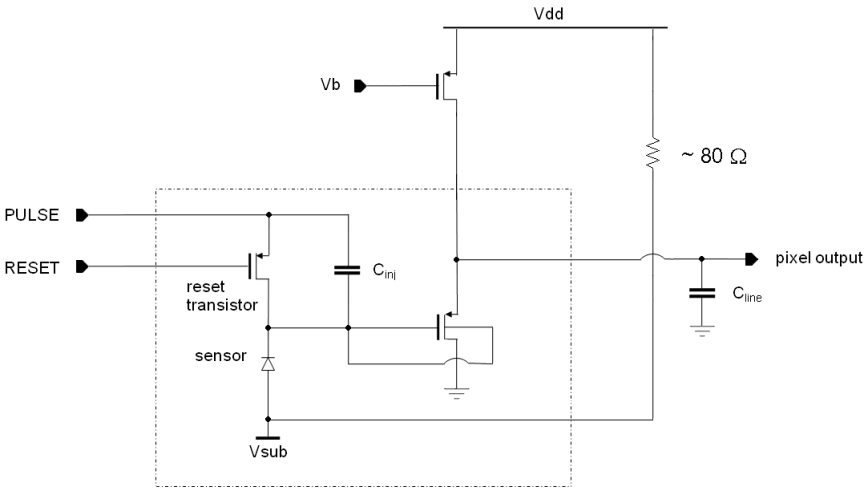

Figure 5.10: Resistive path introduced by the short.

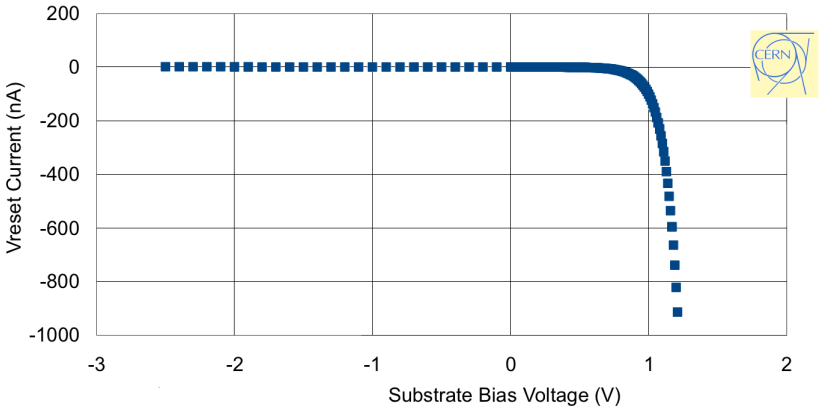

Figure 5.11: Exponential characteristic for breakdown test structures.

At this point we have to note that both in active-reset and in continuous-reset pulsed rows the test pulse is given upon a *capacitive divider* formed by the injection capacitance C_{inj} and the sensor capacitance C_{pix}. The effective voltage on the input transistor gate is given therefore by the relationship

$$V_G = \frac{C_{inj}}{C_{pix} + C_{inj}} V_{PULSE} \quad .$$

Due to the short the sensor capacitance is expected to be orders of magnitude larger than the injection one. Thus, being $C_{pix} \gg C_{inj}$ the signal amplitude seen by the input device will be extremely small, in practice not measureable. For the same reason, any particle hit can not be detected.

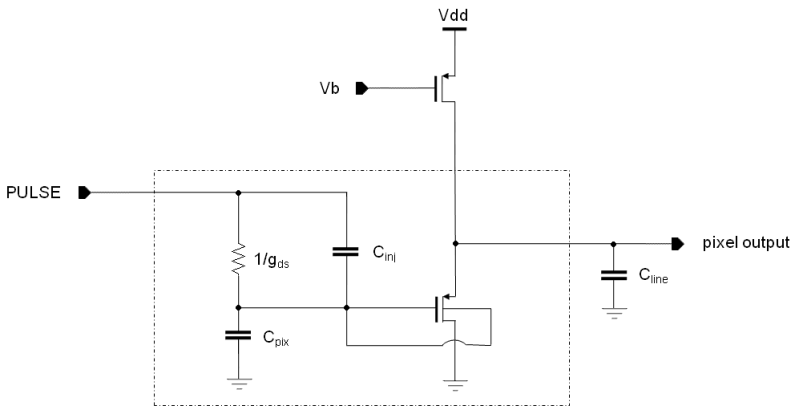

Figure 5.12: Sensor exclusion keeping ON the reset transistor.

The only way to perform measurements and tests is *to exclude* the sensor, although only active-reset rows provide this opportunity. In particular, this can be achieved keeping in saturation the reset transistor for the whole duration of the acquisition time using a longer PIX_RESET signal. As sketched in Figure 5.12 in this case the reset transistor (which works in weak inversion) behaves like a linear resistor $1/g_{ds} \approx 10$ kΩ. Neglecting the little voltage drop through this resistance we can assume that the test pulse is applied directly on the input device gate, excluding the sensor. The drawback is that any characterization of the sensor and physical measurements with sources becomes impossible. Furthermore, a detailed characterization of the integrated read-out electronics chain can be performed for active-reset pixels only.

Before concluding, it is proper to focus and to remark that the above-mentioned issue araised attempting a really *non standard* and *aggressive* layout developed for a non standard and innovative detector.

5.5 Setup characterization

Setup linearity

A correct testing procedure requires a verification of the linearity of the external-chip electronics and a measurement of its overall voltage gain. Hence the first set of measurements presented in this section consists of the calibration curves of the mezzanine read-out and of the characterization of the setup noise, without the chip wire-bonded onto the mezzanine.

A simplified schematic of the external-chip read-out chain, from the matrix output pad to the ADC inside the DAQ system, is shown in Figure 5.13.

As already mentioned, the mezzanine is equipped with a bare minimum standard circuitry. In particular, the OUTMATRIX pad is connected to a first non-inverting operational amplifier (OPAMP) with a closed-loop gain given by $A_V = 1 + R_2/R_1$, determined by the ratio between the feedback and the input resistor. Being $R_1 = R_2 = 10$ kΩ the nominal voltage gain is 2. The following stage is a fully differential amplifier (FDA), which provides the conversion from a single-ended signal to a fully-differential one, in order to reject the common-mode noise. Therefore the difference between the two FDA output signals is fed to the 14 bit ADC inside the DAQ system. The nominal closed-loop voltage gain of the FDA stage is 1/2 between the single-ended input and each one fully-differential output, hence the total gain between the OPAMP input and each FDA output is $2 \times 1/2 = 1$. The overall voltage gain between the OPAMP input and the ADC output is $1 - (-1) = 2$.

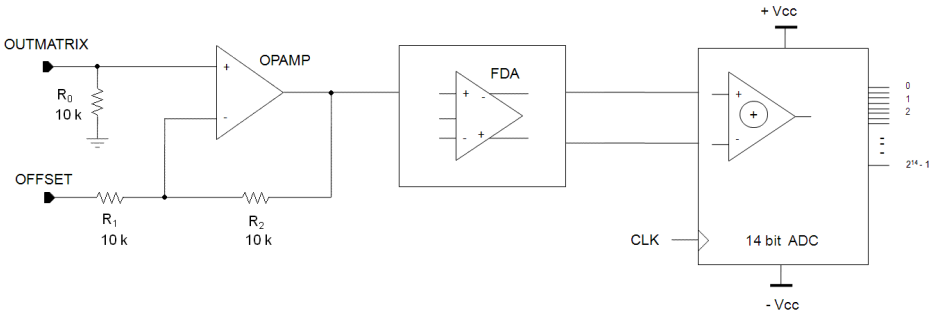

Figure 5.13: Simplified schematic of the external-chip read-out chain.

In Figure 5.14 and 5.15 we present the DC characteristics, obtained respectively by changing the OPAMP offset voltage with a fixed DC input voltage and, vice-versa, by changing the DC input voltage with a fixed OPAMP offset. Note that DC output voltages have been measured directly via software interface by selecting the architecture of matrices M1-M2 that provides 2048 values for any signal or DC voltage applied to the OUTMATRIX pad.
These characteristics ensure the required DC linearity for the external-chip electronics.

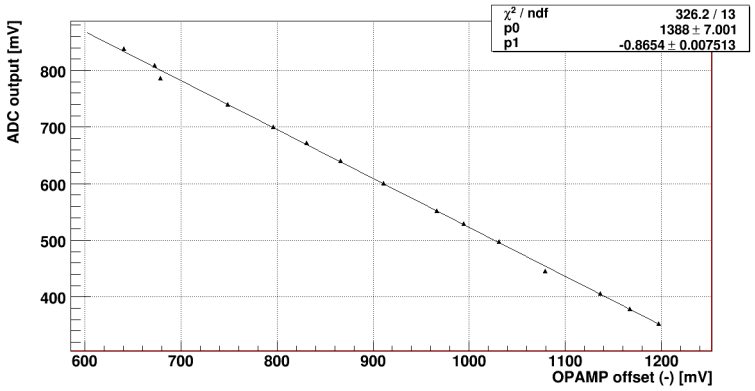

Figure 5.14: ADC output vs. OPAMP offset.

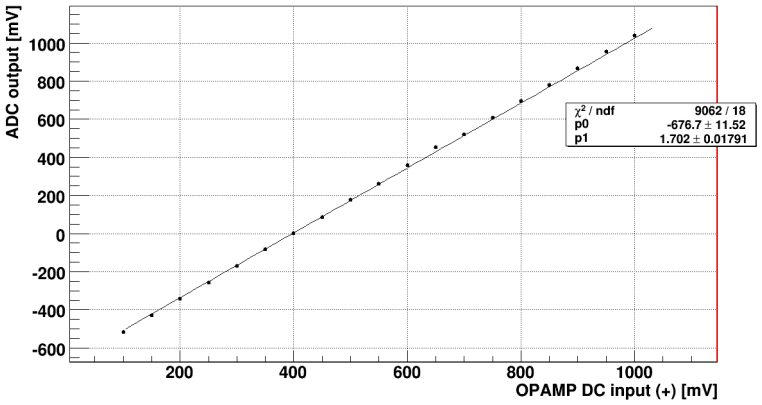

Figure 5.15: ADC output vs. OPMAP DC input (OUTMATRIX pad).

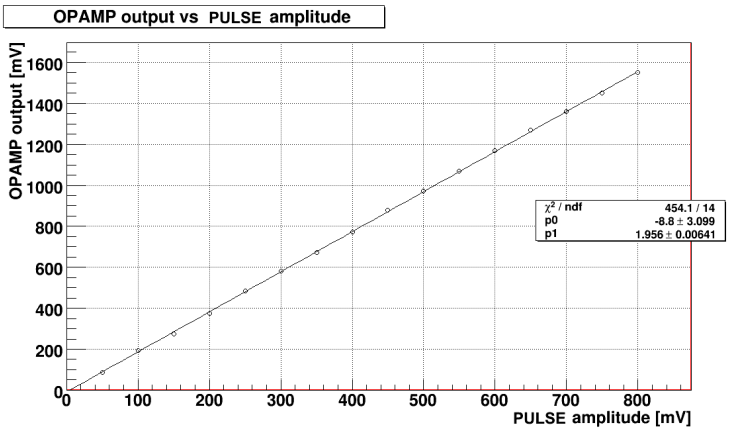

Figure 5.16: OPAMP output vs. PULSE amplitude.

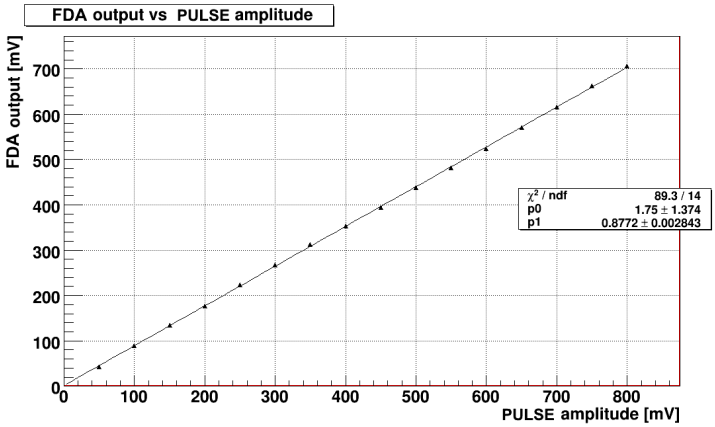

Figure 5.17: FDA output vs. PULSE amplitude.

Gain characteristics are shown instead in Figure 5.16, 5.17 and 5.18. They have been obtained pulsing the OPAMP input and studying device-outputs for different pulse amplitudes. The slope of each characteristic represents the gain between input and output.

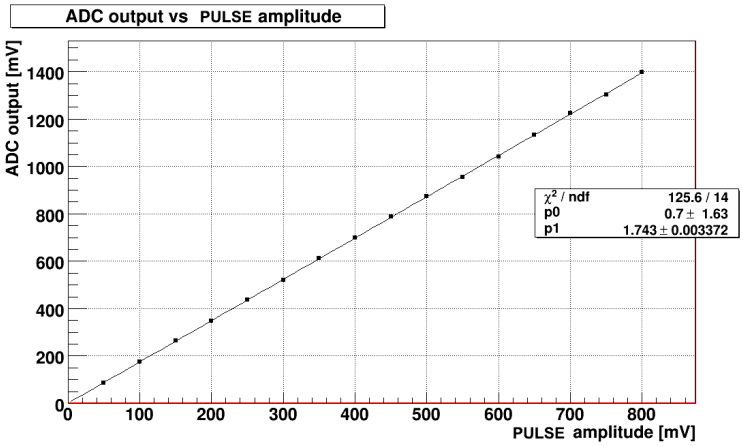

Figure 5.18: ADC output vs. PULSE amplitude.

The measured OPAMP gain is 1.956 ± 0.005, which is in good agreement with the nominal value 2. The slope of the FDA characteristic is instead 0.877 ± 0.003, whereas the nominal gain between the OPAMP input and each FDA output should be $2 \times 1/2 = 1$. Hence the FDA stage exhibits a little signal loss.
The overall voltage gain between the ADC output and the OPAMP input is 1.743 ± 0.003, according with the double of the measured FDA gain, but with a further little signal loss.

Note that OPAMP and FDA outputs are easily accesible with a probe, hence characteristics in Figure 5.16 and 5.17 have been obtained measuring the amplitude of the output pulse with the oscilloscope.
On the other hand, as shown in Figure 5.19 and 5.20 the measurement of the ADC pulse amplitude requires the off-line reconstructuction of the waveform.

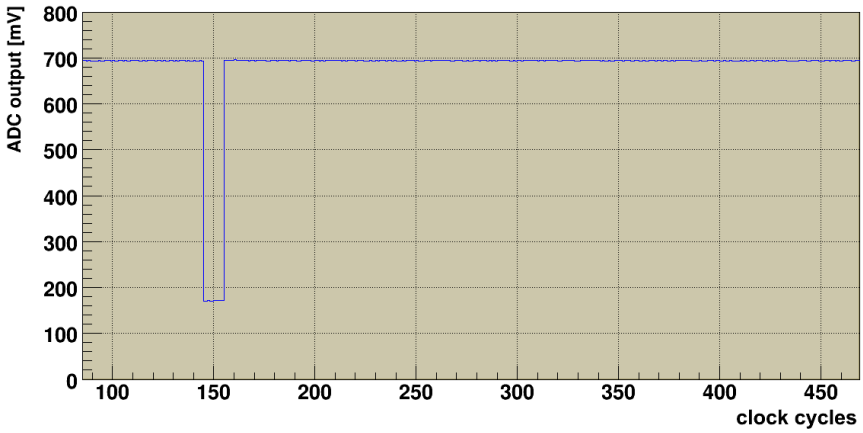

Figure 5.19: Off-line reconstructed pulse.

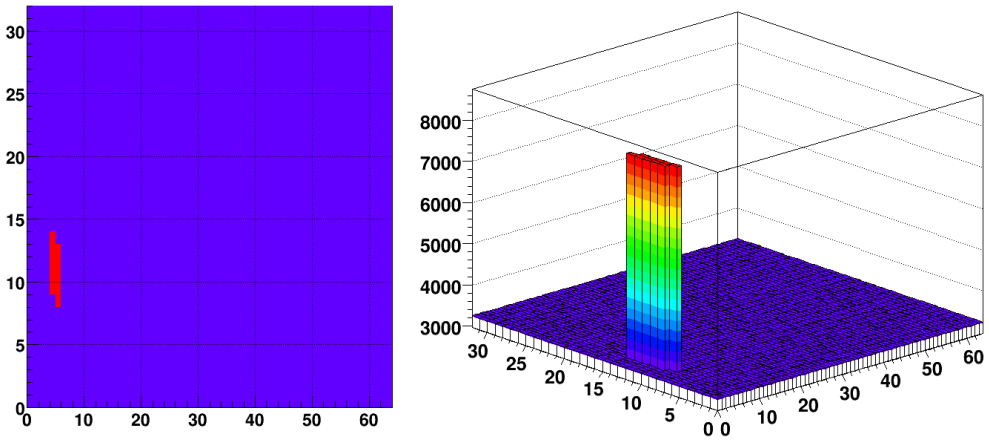

Figure 5.20: Off-line reconstructed pulse in the pixel-map.

Setup noise

A second characterization without a chip wire-bonded onto the mezzanine is the measurement of the read-out chain noise.
As shown in Figure 5.21, although the OPAMP input (the OUTMATRIX pad of the mezzanine) is kept to a certain fixed DC voltage the output sequence of 2048 values provided by the software is a baseline with some fluctuations of about 0.5 mV, due to the thermal noise.
These fluctuations have to be compared with the resolution of the ADC, given by the less significative bit (LSB). Reminding that the device converts a voltage in a integer between 0 and $2^{14} - 1$ and works within a nominal power supply of $\pm V_{CC} = \pm$ 1.15 V we have

$$LSB = \frac{2\ V_{CC}}{2^{14}} = 0.14 \text{ mV} \quad .$$

This value represents the nominal resolution of the ADC.

In order to have some more significant statistics, the measurement of fluctuations has been obtained by processing 100 SHOT files. In particular, one histogram for each acquisition has been filled with all 2048 ADC output voltages, providing a certain RMS. Then, as show in Figure 5.22 a histogram filled with all RMSs provides a mean which can be assumed as a measurement of the overall setup noise. The Gaussian fit gives $\mu \approx 0.35$ mV, hence an uncertainty of at least $0.3 \div 0.4$ mV should be considered for all measurements provided by the ADC.

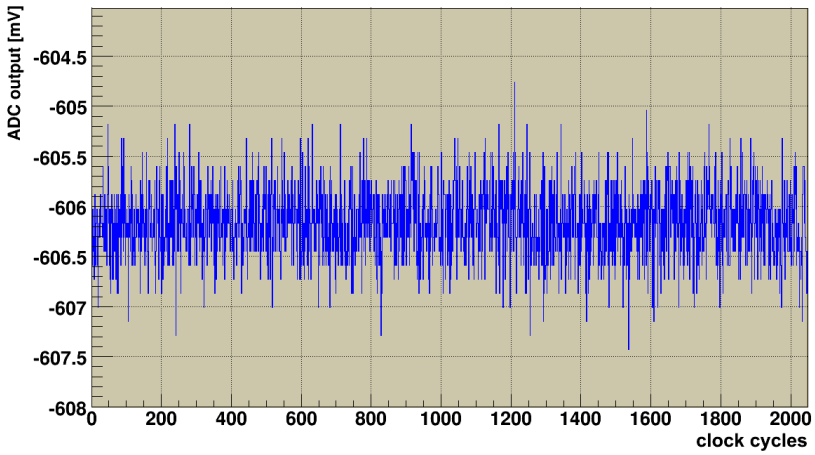

Figure 5.21: ADC serial output for a certain fixed OPAMP input voltage.

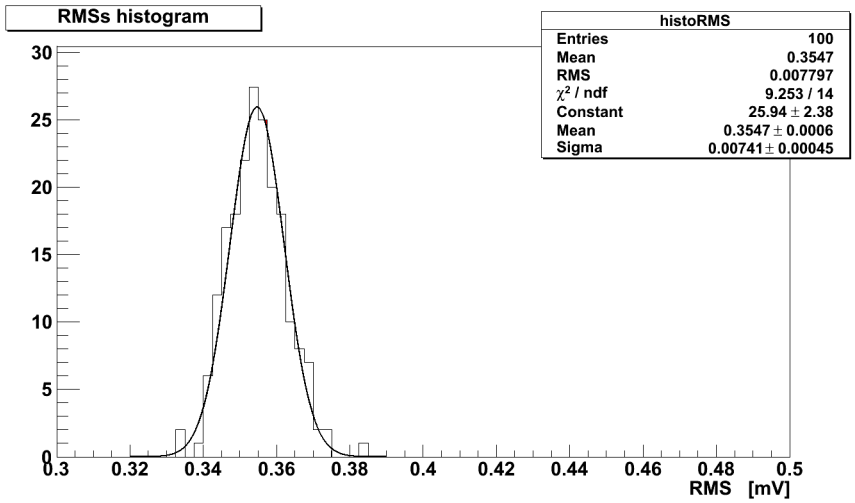

Figure 5.22: Histogram of RMSs with Gaussian FIT.

5.6 Matrix 1-2 CORE part characterization

In this section tests and measurements performed on matrix M1 are discussed. The matrix is equipped with a MAPS-like analog read-out, as described in 4.4. We remind that only active-reset sensors can be excluded keeping in saturation the reset transistor for all the duration of the acquisition time, as sketched in Figure 5.23. Hence, only the first pulsed row allows a characterization of the front-end electronics. In particular, the PIX_RESET signal begins a clock cycle after the START rising edge and ends a clock cycle before the START falling edge. The RESET_DFF (at least 1 μs) resets D-Flip/Flops of the shift register. The minimum duration of MEM1 and MEM2 signals is one clock cycle. MEM1 should sample the first voltage a few clock cycles after the PIX_RESET rising edge, whereas the delay of MEM2 with respect MEM1 is tunable. Of course, in order to sample the PULSE low level, MEM2 must fall inside the PULSE width.
The PULSE amplitude varies in the $0 \div 800$ mV range, with a maximum high level of 800 mV. On the other hand, the time width of the PULSE can not be too large, avoiding that the PULSE low level behaves like a constant DC level for the injection capacitor.

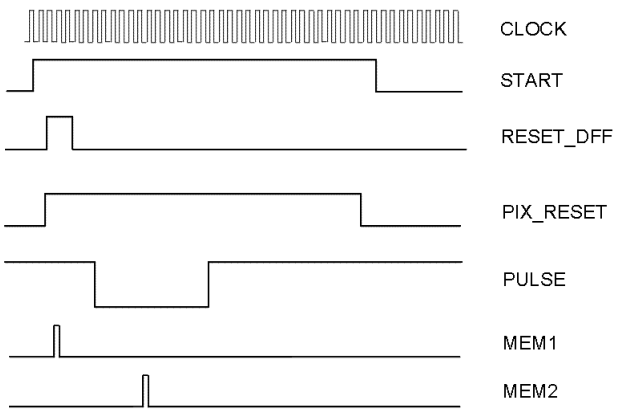

Figure 5.23: Signal timing for matrix M1 characterization.

After a description of the matrix output and of the PULSE recostruction moving MEM2, a detailed characterization of the read-out electronics with source followers (SFs) is given. Furthermore, DC and gain measurements have been performed, studying also frequency behaviour and reverse bias dependences. Finally, an estimation of the pixel capacitance is discussed.

Matrix output

The matrix CORE part serial output can be probed directly with a oscilloscope on the OUTMATRIX pad or reconstructed off-line using the specific tool.
The reconstructed sequence is depicted in Figure 5.24 (without PULSE) and in Figure 5.25 (with PULSE).

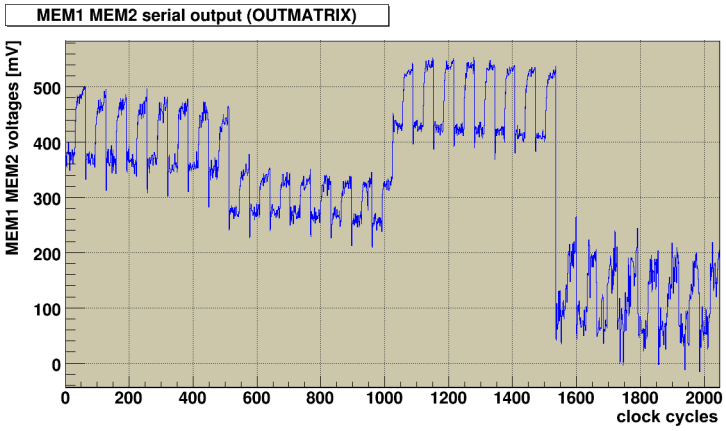

Figure 5.24: OUTMATRIX serial output without PULSE.

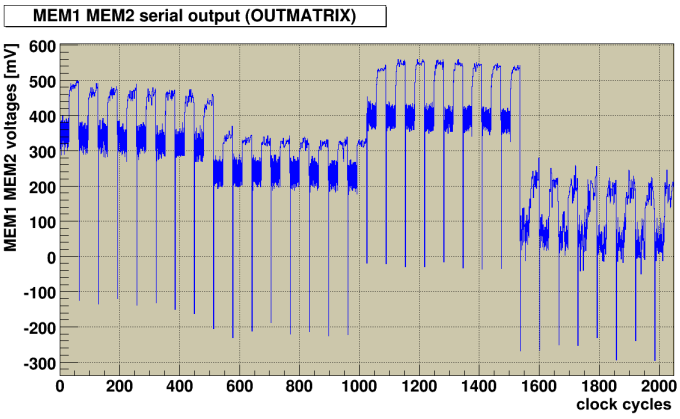

Figure 5.25: OUTMATRIX serial output with PULSE.

As described in Chapter 4 the read-out of the matrix is serial and contains the V_{MEM1} V_{MEM2} sequence of all 1024 pixels in the CORE part. Therefore in the plots we can recognize the entire CORE part structure, with two voltages stored for the first pixel (0), two voltages for the second one (1) and so on.

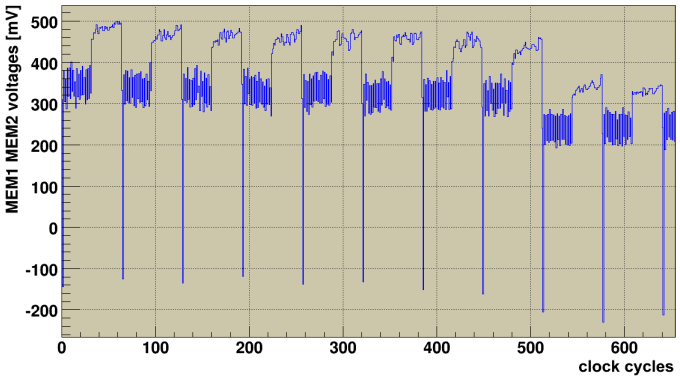

Figure 5.26: First macro-column: 8 columns with 16 active-reset + 16 continuous-reset each one

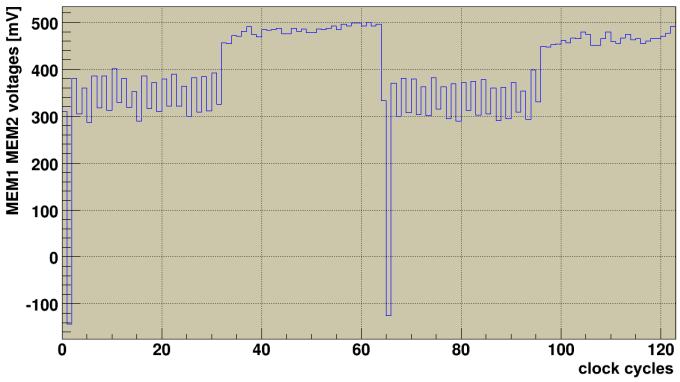

Figure 5.27: First column: 16 active-reset + 16 continuous-reset.

In particular, in the waveform structure we can firstly recognize 4 main parts, corresponding to the matrix vertical segmentation in 4 macro-columns with different types of input device (i.e. two sizes of thin oxide PMOS, thick oxide PMOS and NMOS).

Then each macro-column contains 8 columns of 32 pixels each one, as shown in the first zoom in Figure 5.26.
Each column contains 16 active-reset pixel and 16 continuous-reset. For instance, in the second zoom in Figure 5.27 we can recognize 32 pixels of the first column, with the V_{MEM1} V_{MEM2} sequence for the first 16 active-reset pixels (32 values) followed by 16 continuous-reset outputs (further 32 values).

Note that if the PULSE is applied, in the waveform we can also observe pixels of the first active reset pulsed row. They appears with V_{MEM2} negative spikes for pixels (0), (32) etc.
However, due to the large capacitance of the not depleted substrate, there are no spikes for pixels of the continuous-reset pulsed row.

Furthermore, filling a 2D histogram with the V_{MEM1} V_{MEM2} sequence we obtain the off-line reconstruction of the matrix-map provided by the acquisition interface, as shown in Figure 5.28.
In particular, in the left 32 $\times$ 64 map we can easily recognize the V_{MEM2} values of the first active-reset pulsed row. In the right 32 $\times$ 32 map the $V_{MEM1} - V_{MEM2}$ differences have been plotted, and we observe the first active-reset pulsed row again.

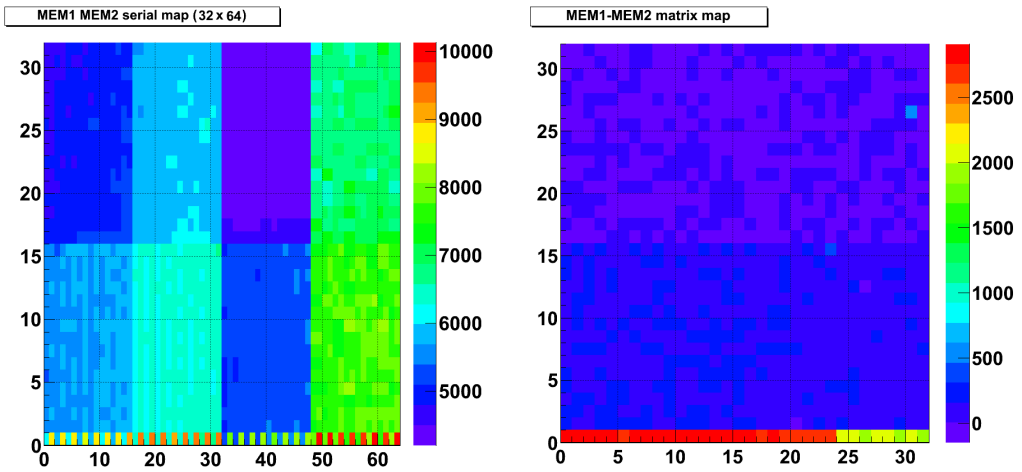

Figure 5.28: Matrix maps off-line recostruction.

Reconstruction of the PULSE moving MEM2

According to the signal timing shown in Figure 5.23, a simple test can be performed moving the MEM2 signal away from a fixed MEM1. The goal is to obtain an off-line reconstruction of the input waveform by sampling with MEM2 different values of the PULSE, as depicted in Figure 5.29.

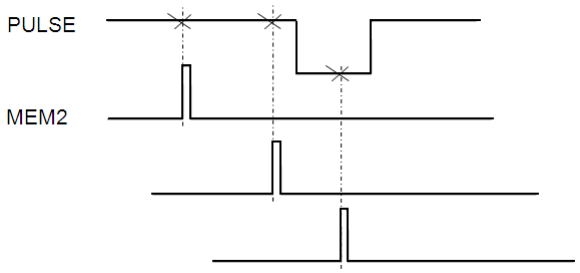

Figure 5.29: Reconstruction of the PULSE moving MEM2.

A PULSE of 400 mV of amplitude and 50 μs of width has been used, working at 100 kHz of clock frequency (i.e. 10 μs for each clock cycle). Furthermore, no reverse bias has been applied to the substrate.
The ROOT tool provides the characteristics for all pulsed pixels, both active- and continuous-reset. However, only a sigle representative characteristic for each input device is presented (i.e. the fourth pixel of each macro-column).

As a matter of fact, only input transistors of the active-reset pulsed row received the PULSE, as shown in Figure 5.30. Thus the sensor capacitance has been excluded, according to predictions.
On the other hand, as already mentioned, continuous-reset input devices receive an insignificant PULSE, because the voltage on the input device gate is driven by the capacitive divider relationship described in 5.4. Therefore no PULSE has been reconstructed for the continuous-reset pulsed row, as shown in Figure 5.31.

Note that although this test may seem something trivial, actually it represents a direct proof of the severe constraint introduced by the short in the guard.

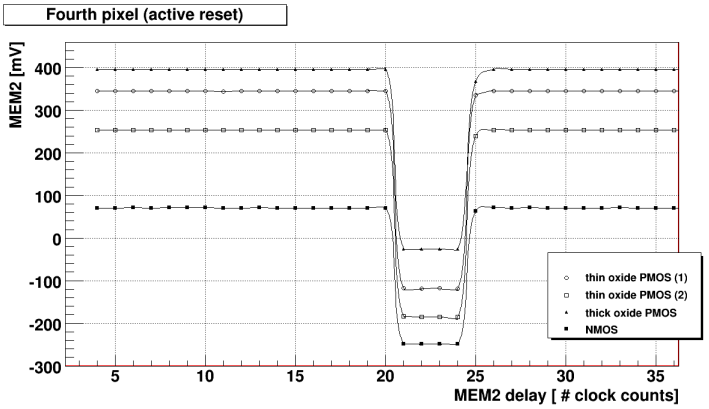

Figure 5.30: Reconstructed PULSE for active-reset pulsed row devices.

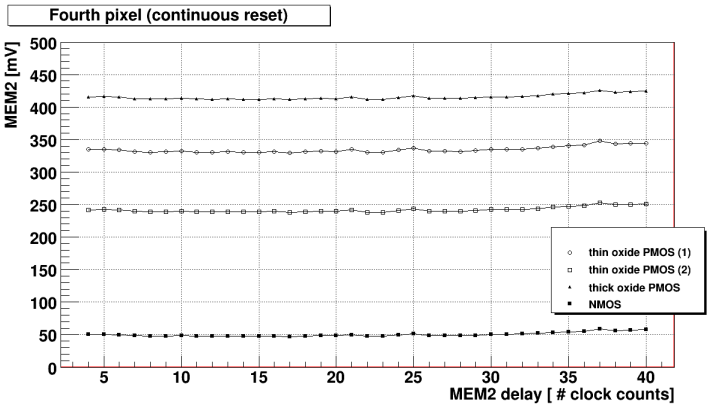

Figure 5.31: No PULSE reconstructed for continuous-reset pulsed row devices.

Source followers (SFs) characterizations

A detailed characterization of the matrix M1 read-out electronics is now given. DC characteritics are fundamental in determining the right gate operating voltage for the input devices.
A measurement of the source followers (SFs) voltage gain and a verification of the devices homogeneity is required, validating the 90 nm read-out electronics. Furthermore, frequency and reverse bias behaviours are discussed.
All plots have been extracted from the acquisition interface using the dedicated off-line tool. Each plot contains V_{MEM2} values or $V_{MEM1} - V_{MEM2}$ differences as a function of a certain parameter. As already mentioned, only a representative characteristic for each input device is presented, except for the homogeneity verification.

First characteristics have been obtained decreasing a DC voltage applied on the PULSE input pad, from 900 mV to 50 mV. In this way a DC analysis can be performed for the active-reset pulsed row devices, studying DC output voltages as a function of the input DC level. Note that neglecting very little differences (below 1 mV) due to leakage currents in CMOS switches the DC output voltage is $V_{MEM1} = V_{MEM2}$. Moreover, measurements have been repeated using slightly different reverse biases.

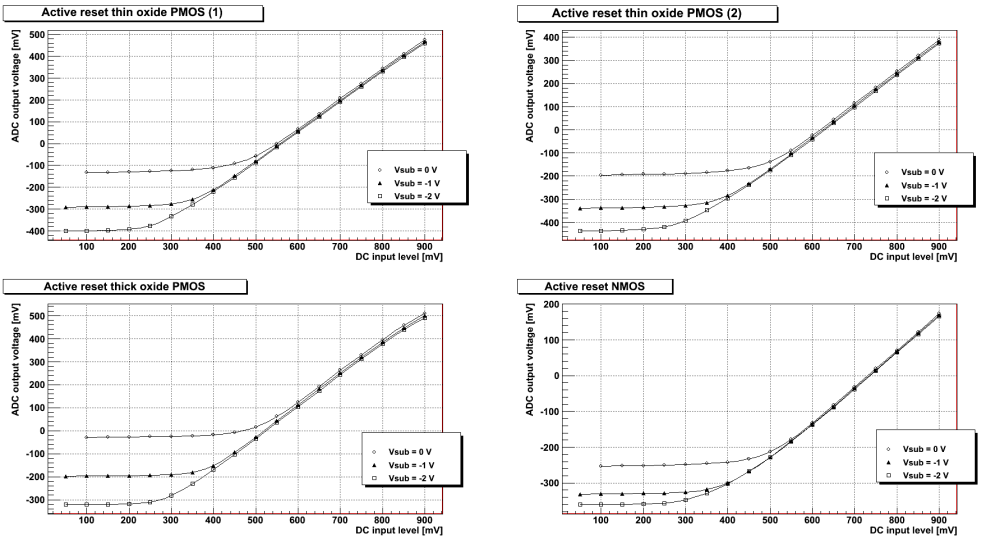

Figure 5.32: DC characteristics for slightly different reverse biases.

The DC input voltage drives the source of the PMOS reset transistor. Characteristics in Figure 5.32 show that decreasing the input DC voltage the reset device tends gradually to switch off. Hence, the output voltage initially decreases linearly and then saturates to a certain constant DC level, because when the reset transistor is off the gate of the first source follower is fixed by the voltage drop of the collection electrode. Increasing (in modulus) the reverse bias V_{SUB} increases the extension of the linear region. Therefore biasing the substrate the reset transistor off-voltage increases.
Of course the proper input DC operating point must be choosen within the linear region, at least grater than 600 mV if no reverse bias is applied. In particular, the PULSE high-level has been set to 800 mV for all measurements.

We now discuss the measurement of the source followers voltage gain, introducing the second set of characteristics.
In particular, the input-output behaviour has been obtained plotting the $V_{MEM1} - V_{MEM2}$ differences versus different PULSE amplitudes. Of course, the MEM2 signal must fall inside the PULSE width, in order to sample the low-level of the waveform. Characteristics for the active-reset pulsed row are shown in Figure 5.33. In this case each canvas contains 8 plots, monitoring all pixels with different input transistors.
The trend is the same for all pixels, with a linear increase followed by a saturation. When the PULSE amplitude is too large (above 300 mV) the proper DC operating point of the input SF changes, hence the characteristics saturate.
The slope of each characteristic represents the overall voltage gain, from the input device to the ADC output. Therefore, after a previous measurement of the voltage gain of the external-chip read-out chain, it is possible to determine the source followers voltage gain. In particular, $0.87 \div 0.89$ for PMOS input devices and 0.76 for NMOS have been obtained. These values are in agreement with the amplification of a standard source follower. Furthermore, all devices of each macro-column have the same voltage gain (within the uncertainties provided by linear fits), ensuring the homogeneity of these 90 nm SFs.
We can observe that NMOS input transistors exhibit a voltage gain lower than PMOS ones, according to the *body effect* which affects NMOS devices [10]. Furthermore, the saturation occurs for ≈ 300 mV, whereas PMOS devices saturate for a PULSE amplitude ≈ 400 mV. This is in agreement with the fact that both PMOS and NMOS input devices have the same building block at the periphery of the matrix, with NMOS source followers. Hence a NMOS input device followed by another NMOS source follower leads to a reduced output swing.

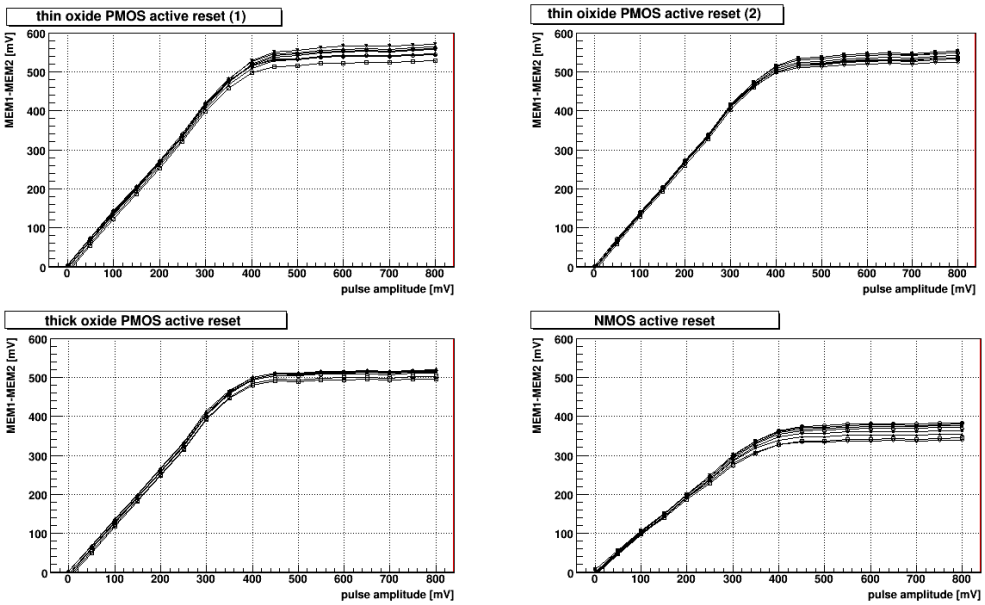

Figure 5.33: $V_{MEM1} - V_{MEM2}$ vs. PULSE amplitude (active-reset pulsed row).

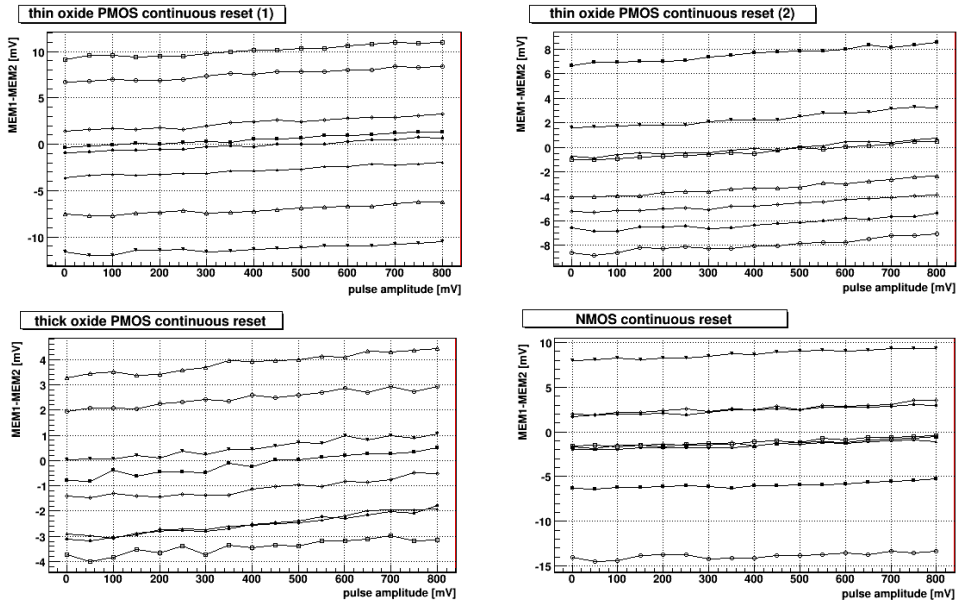

Figure 5.34: $V_{MEM1} - V_{MEM2}$ vs. PULSE amplitude (continuous-reset pulsed row).

Continuous-reset characteristics (8 plots for each canvas again) are shown in Figure 5.34. According to the short, due to the large capacitance of the not depleted substrate the PULSE amplitude seen on the gate of continuous-reset input devices is insignificant.
We can recognize a slight linear increase, hence a certain amplification is performed. However, these characteristics are heterogeneous.

The following characterization is a study of the SFs voltage gain as a function of the reverse bias V_{SUB}. Representative characteristics for the active-reset pulsed row are shown in Figure 5.35.
In order to avoid chip damages, a maximum reverse bias of -2 V has been applied. All plots show the same previous behavior, with a linear increase followed by a saturation if the PULSE amplitude becomes too large.
The voltage gain is independent of the reverse bias applied, as predictable. On the other hand, increasing the reverse bias (in modulus) increases the extension of the linear region. Hence the saturation voltage increases (e.g. from 300 mV with $V_{SUB} = 0$ V to 500 mV with $V_{SUB} = -2$ V for PMOS input devices). This reverse bias dependence can be attributed to the matrix short. Reasonably, if the substrate is reverse biased then parasitic currents through the resistive path increase, hence the voltage drop between the n-well collection electrode and the substrate changes.

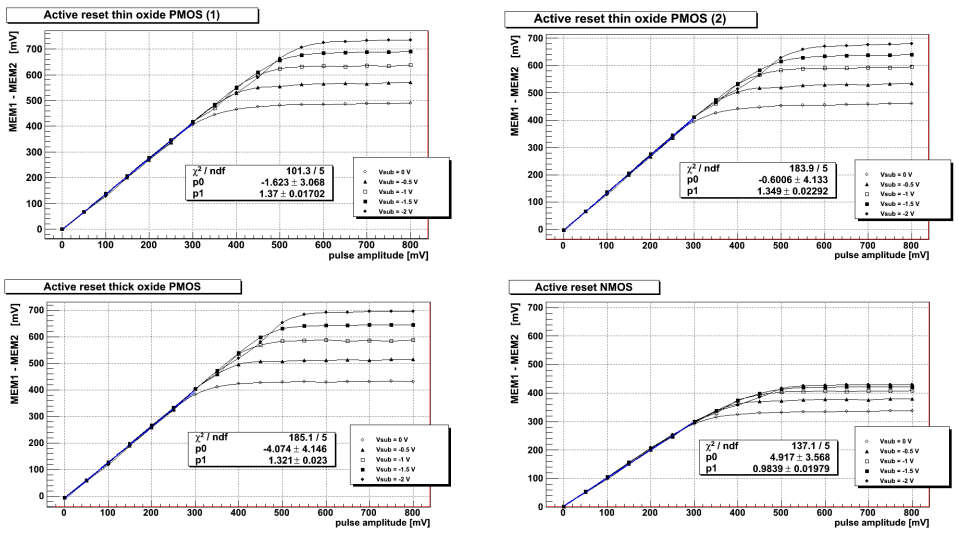

Figure 5.35: $V_{MEM1} - V_{MEM2}$ vs. PULSE amplitude for different slight reverse biases.

At the end, a frequency analysis can be performed studying the SFs voltage gain as a function of the CLOCK frequency. All characteristics have been obtained with a fixed reverse bias $V_{SUB} = -1$ V, varying the frequency value via software from 100 kHz to 3.12 MHz. As shown in Figure 5.36 the voltage gain decreases with the CLOCK frequency.
This represents another consequence of the not depleted sensor. In fact, for a certain fixed number of clock cycles between MEM1 and MEM2, increasing the CLOCK frequency decreases the distance between MEM1 and MEM2. Due to the large capacitance C_{pix} of the not depleted substrate the PULSE signal is filtered by a RC low-pass filter (see later). Hence the PULSE has smooth falling and rising edges and the voltage sampled by MEM2 decreases increasing the CLOCK frequency, leading to a lower voltage gain.

This result introduces the estimation of the pixel capacitance, described in the next section.

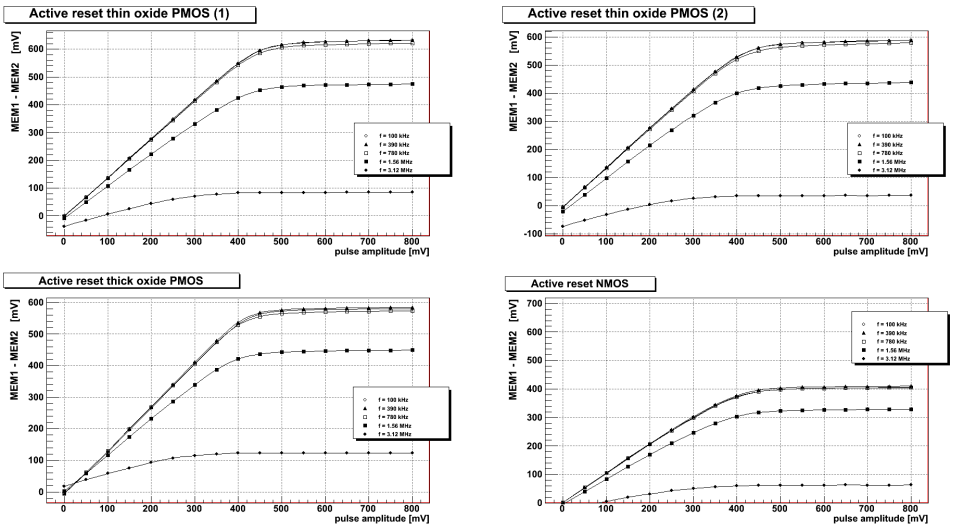

Figure 5.36: $V_{MEM1} - V_{MEM2}$ vs. PULSE amplitude for different CLOCK frequencies.

Estimation of the pixel capacitance

We conclude the matrix M1 characterization describing a test which provides an estimation of the pixel capacitance. As described in 5.4, this value is expected to be much larger than the injection capacitance.

In order to better understand the measurement procedure, we reintroduce in Figure 5.37 the equivalent circuit of an active-reset pixel cell. In particular, keeping in saturation the reset transistor for the entire duration of the START, the device in saturation behaves like a linear resistor $R_1 = 1/g_{ds}$ due to short channel effects.
A simplified schematic is depicted in Figure 5.38, in which the input source follower has been replaced by a simple voltage buffer. The resistor R_2 represents the total impedance of the load driven by the input device, whereas C_{line} is the parasitic capacitance of the transmission line.

Although the external PULSE is a signal with sharp rising and falling edges, the waveform sampled by MEM1 and MEM2 is expected to have smooth transitions due to parasitc capacitances. In particular, the PULSE is fed to a RC low-pass filter and there is no current through the gate of the first input transistor. Hence the buffered voltage output is fed to a second RC low-pass filter. The signal sampled by MEM1 and MEM2 is therefore a PULSE which undergoes two integrations performed by two buffered RC low-pass filters.

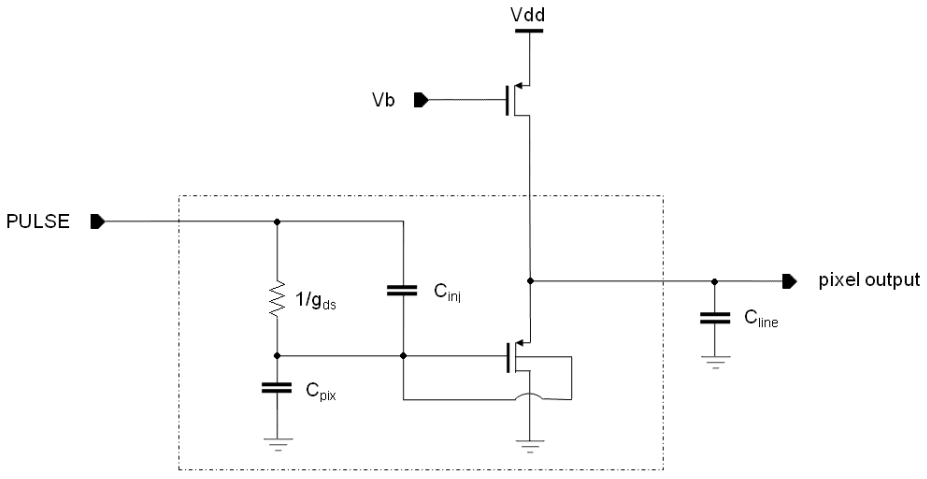

Figure 5.37: Active-reset pixel cell with the PMOS reset transistor in saturation for the entire duration of the START.

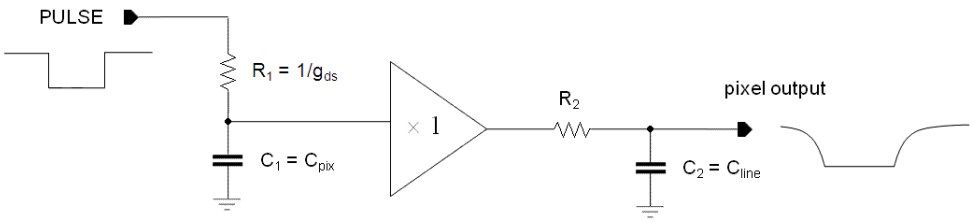

Figure 5.38: A simplified schematic of an active-reset pixel cell. The reset transistor behaves like a linear resistor and the input source follower has been replaced by a simple voltage buffer.

Using Laplace transformations we can predict the analytical expression of the output waveform. The transfer function of the circuit is the convolution of two RC low-pass transfer functions in the time domain. Hence a product of transfer functions in the complex frequency $s = \sigma + j\omega$ domain is obtained:

$$\int_{0^-}^{t} d\tau \; h_1(\tau) h_2(t-\tau) \quad \Rightarrow \quad H(s) = H_1(s)\, H_2(s)$$

In particular,

$$\begin{aligned} H_1(s)\, H_2(s) &= \frac{1/sC_1}{R_1 + 1/sC_1} \, \frac{1/sC_2}{R_2 + 1/sC_2} \\ &= \frac{1}{1+s\tau_1} \, \frac{1}{1+s\tau_2} \end{aligned}$$

with $\tau_1 = R_1 C_1$ and $\tau_2 = R_2 C_2$ the time constants. The PULSE edges are voltage steps, thus

$$v_{in}(t) = k\, u(t) \quad \Rightarrow \quad V_{in}(s) = \frac{k}{s}$$

while the output one in the complex frequency domain is

$$V_{out}(s) = V_{in}(s)\, H(s) = \frac{k}{s} \, \frac{1}{\tau_1(s+1/\tau_1)} \, \frac{1}{\tau_2(s+1/\tau_2)} \quad .$$

Finally, we obtain the output voltage in the time domain using the inverse Laplace transformation (e.g. using the method of residues), which gives

$$v_{out}(t) = k \left[1 - \frac{1}{\tau_1 - \tau_2} \left(\tau_1 \, e^{-t/\tau_1} + \tau_2 \, e^{-t/\tau_2} \right) \right] \quad .$$

The idea of the measurement has been to perform a fine scan of the PULSE rising and falling edges. Then experimental points can be fitted using the $v_{out}(t)$ function, extracting an estimation for $C_{pix} = C_1$.
Actually, this can not be achieved by moving the MEM2 signal, because it can be shifted via software with a minimum step of one clock cycle only. The duration of the PULSE edges is below 1 μs, hence working for instance with a standard 100 kHz frequency a minimum time step of 10 μs is too large.
For this reason, as sketched in Figure 5.39 measurements have been obtained by moving the PULSE with time steps of 5$\div$10 ns, keeping MEM2 fixed instead.

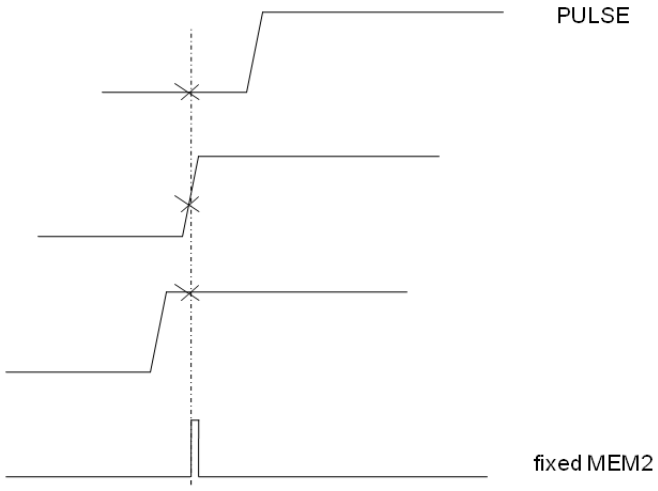

Figure 5.39: Fine scan of the PULSE rising edge.

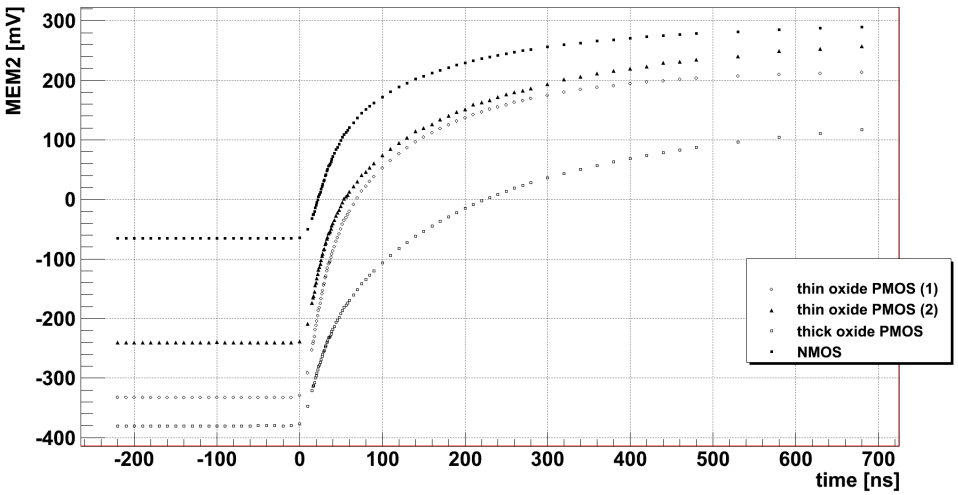

Figure 5.40: Rising edges scan - experimental data.

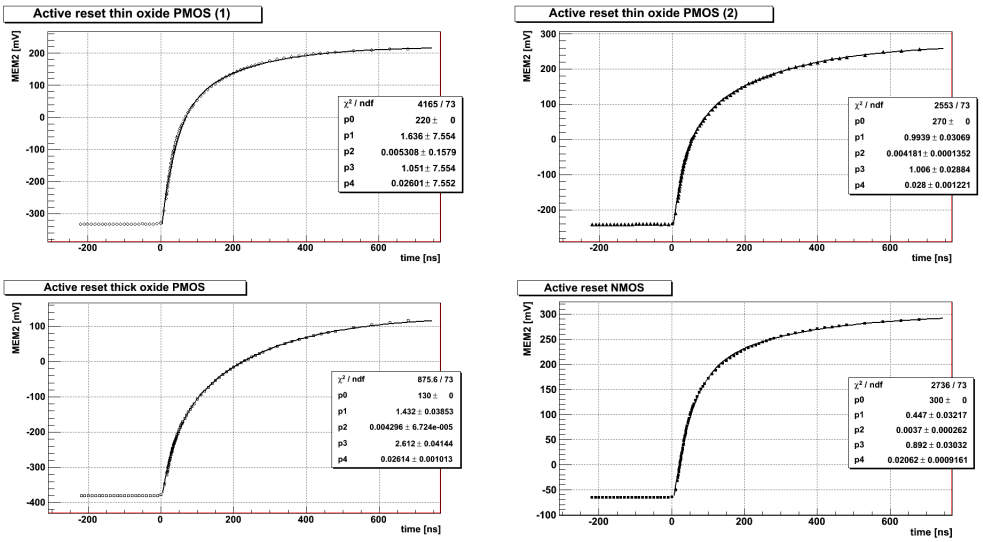

Figure 5.41: ROOT fits.

Representative characteristics with a fine scan of the PULSE rising edge are shown in Figure 5.40. In particular, V_{MEM2} values are plotted versus the delay between the MEM2 rising edge and the sharp PULSE one, measured with the oscilloscope.
In Figure 5.41 data have been fitted using the simplified function

$$v_{out}(t) = p_0 \left[1 - p_1\, e^{-p_2 t} - p_3\, e^{-p_4 t}\right] \ ,$$

neglecting coefficients constraints of the theoretical output waveform. Thus, fit parameters provide the time constants as $\tau_1 = 1/p_2$ and $\tau_2 = 1/p_4$. Consistent values have been obtained for all characteristics, with $\tau_1 \approx 200\,\text{ns}$ and $\tau_2 \approx 38\,\text{ns}$.
Assuming that the PMOS reset transistor behaves like a resistor with $R_1 = 1/g_{ds} \approx 10\ \text{k}\Omega$ we obtain for the pixel capacitance

$$C_{pix} = \frac{\tau_1}{R_1} \approx 20\,\text{pF} \ .$$

According to expectations, this value is much larger than the injection capacitance $C_{inj} = 1$ fF (nominal value).
This measurement confirms that $C_{pix} \gg C_{inj}$ for a no reverse-biased substrate. Continuous-reset pixels always exhibit this enormous capacitance at the gate of the input device. Therefore we never observed the PULSE in the continuous-reset pulsed row and no particle hit is detectable.

5.7 Matrix 3-4 CORE part characterization

In the second part of this Chapter tests and measurements performed on a matrix M3 are discussed. We remind that matrices 3-4 incorporate a different version of the read-out electronics, with the input transistor AC coupled to a voltage amplifier (PREAMP) followed by a comparator (DISC). The bare minimum digital part provides a simple *binary* serial read-out based on D-Flip/Flops (DFFs), registering for each pixel if a transition in the comparator occours.

As depicted in Figure 5.42 the signal timing between CLOCK, START, RESET_DFF and PIX_RESET is the same described in 5.6. Of course, MEM1 and MEM2 are meaningless for matrices 3-4. The RESET_DFF signal is essential, because at first sets to 0 all DFFs outputs. The wide PIX_RESET signal excludes the sensor capacitance for active-reset pixels. Although in figure a PULSE is shown, we report beforehand that no PULSE has been observed during these tests, even for the pixels of the active-reset pulsed row.

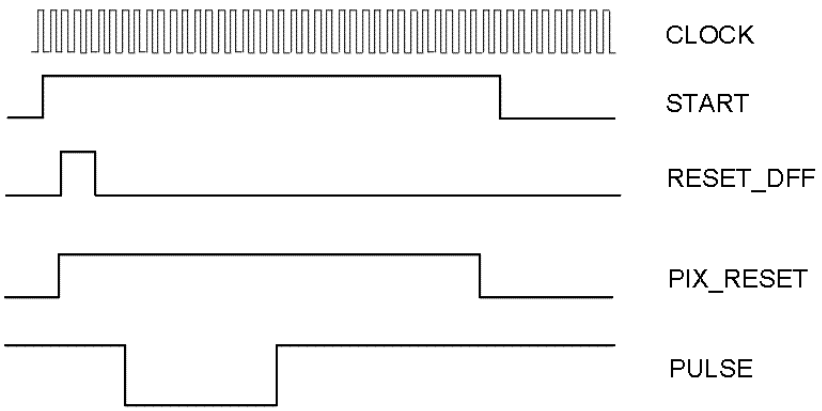

Figure 5.42: Signal timing for matrix M3 characterization.

After a description of the matrix output, noise and thresholds homogeneity studies are discussed. At the end, some bias characteristics are presented, in order to find proper DC operating conditions for PREAMPs and DISCs.

Matrix output

Raw data provided by the software interface for matrices 3-4 contain sequences of 1024 *binary* values 1/0. These logic voltages represent DFFs outputs. Due to the external-chip read-out electronics, CMOS digital levels undergo a shift of 300 mV and they are amplified by the gain of the read-out chain. In particular, in the following, 1 corresponds to about 1.6 V and 0 to 300 mV.
We stress here that the binary information provided by each DFF is if the relative DISC registers/does not register a *transition* with respect to the threshold voltage V_{TH}, as sketched in Figure 5.43.

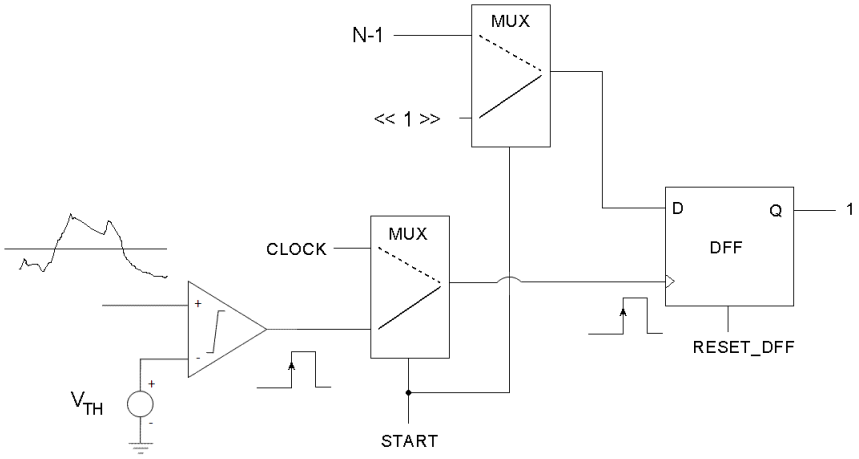

Figure 5.43: Binary read-out for matrices M3-M4.

When START is high the output is 1 if the DISC produces a digital output pulse, providing a clock rising edge for the DFF. This means that some *signal* (physical or parasitic) which intercepts V_{TH} is required. In contrast, input DC levels or signals above or below V_{TH} yield to constant output voltages. Hence without a rising edge the DFF output remains 0.

As shown in Figure 5.44, after the conversion of SHOT and PED files into ASCII files, the off-line reconstruction of the DFF serial output is obtained with a specific tool. The same waveform can be probed on the OUTMATRIX pad with the oscilloscope. Moreover, filling with the same sequence a 2D histogram we obtain the 32 $\times$ 32 CORE part map provided by the acquisition interface, as depicted in Figure 5.45. Note that a red cell corresponds to 1, a blue one to 0.

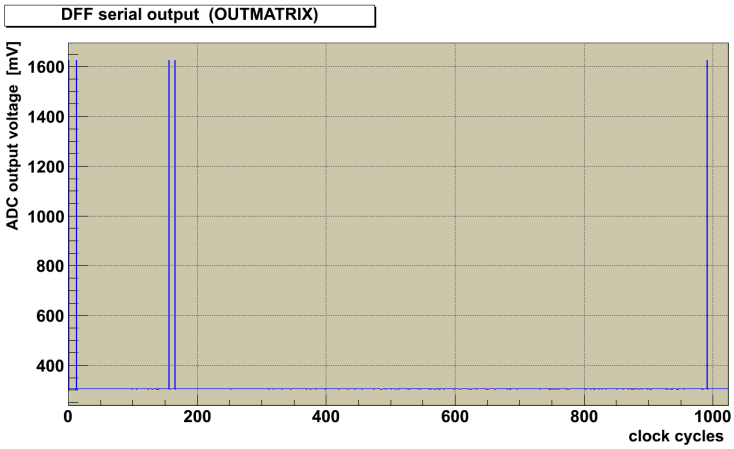

Figure 5.44: Off-line reconstruction of the DFF serial ouput.

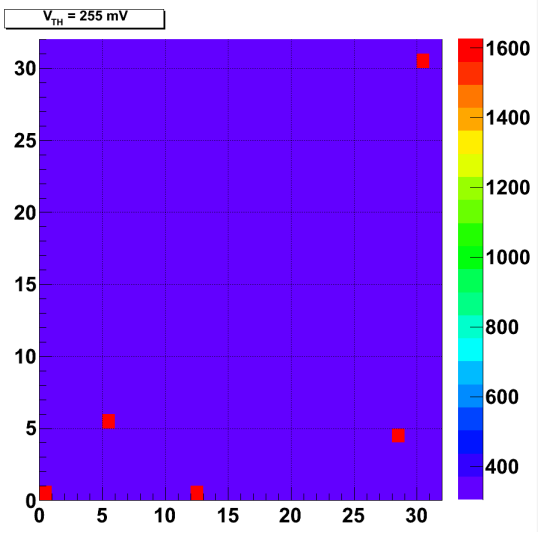

Figure 5.45: Off-line reconstruction of the matrix-map.

Threshold scan and noise

The first test which has been performed is a verification of the matrix output as a function of the DISC threshold voltage V_{TH}. An external Keithley voltage source provided the threshold value to the specific V_{TH} gate on the test PCB.
It is expected that without a physical signal from a pixel cell the respective DISC should not produce a digital output pulse. Hence the DFF output should be 0, because no transition occurs.
Nevertheless, by varying the threshold voltage in the $0 \div 700$ mV range, the front-end register some transitions. In particular, each DFF of the matrix produces a 1 within a certain V_{TH} range. For instance, working with nominal bias conditions (described later) transitions occur in the $250 \div 370$ mV threshold range, as shown in the set of maps in Figure 5.46. On the other hand, if V_{TH} is too low or exceeds a certain maximum value, all DFFs outputs become 0.
Therefore, even if with a certain *dishomogeneity*, all comparators produce a digital output pulse, allowing DFFs outputs to be 1.

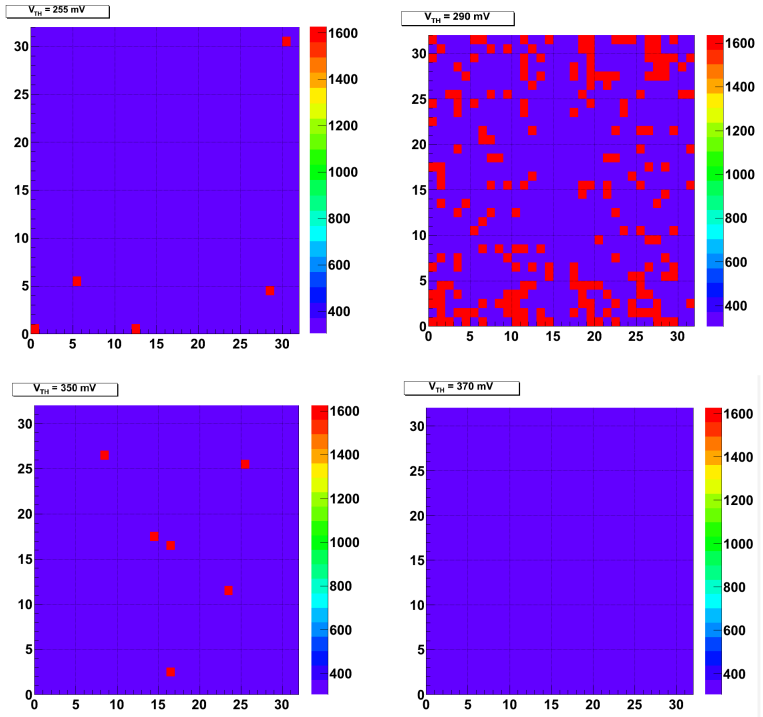

Figure 5.46: Different off-line reconstructed maps increasing V_{TH}.

This behaviour can be explained assuming that a parasitic signal is superimposed to the baseline. Thus, some *noise* affects DISCs inputs.
Reasonably, this noise is due to some parasitic signal injected by the digital electronics into the analog one. Most likely the aggressor signal is the CLOCK, which is the only digital signal always active. Note that typically the noise of a digital circuit is much larger than an analog one, because digital electronics work in the volt range, whereas analog circuits involve signals with a maximum output swing of tens/hundreds of mV.

An off-line analysis of each DFF output as a function of the threshold voltage can be performed. Both SHOT values (stored after a single acquisition) and PED values (averages of 32 consecutive acquisitions) have been plotted, by varying V_{TH} from 250 to 370 mV with a step of 1 mV. In Figure 5.47 and 5.48 are shown respectively SHOT and PED characteristics for a representative DFF output.
When the threshold voltage V_{TH} is below the noise signal there are no transitions in the DISC. Hence the DFF output is 0 (as previously mentioned 300 mV) due to the reset performed at first by the RESET_DFF signal. On the other hand, when the threshold voltage reaches the noise the DISC commutes and produces a digital output pulse. Thus the DFF output becomes 1 (about 1.6 V). This happens for all V_{TH} values which intercepts the noise above the baseline, therefore in the plot we have a plateau. If the threshold exceeds the noise there are no more transitions. The DISC output flips to a continuous 1.2 V logic level and the DFF output remains to 0 again. The width of the characteristic (about 20 mV in Figure 5.47) represents the amplitude of this parasitic signal.

Furthermore, something interesting occurs in rising and falling edges of characteristics. Edge voltages obtained by using PED acquisitions are values between 0 and 1, i.e. no more logic values. This behaviour can be attributed to some ≈ 1 mV *thermal noise* which superimposes to the main parasitic signal.
As sketched in Figure 5.49, if the threshold voltage intercepts some thermal noise the DFF output is indeterminate. Hence PED voltages are averages of one by one logic values, leading at the end to no more logic levels. However, these means are closer to 1 or to 0 depending on the number of individual 1s and 0s.
The same behaviour occurs when the threshold voltage is very close to the maximum of the main parasitic signal, which is expected to be affected by the same thermal noise. Also the spike in the SHOT characteristic in Figure 5.47 is a residual of the DFF indeterminate output.

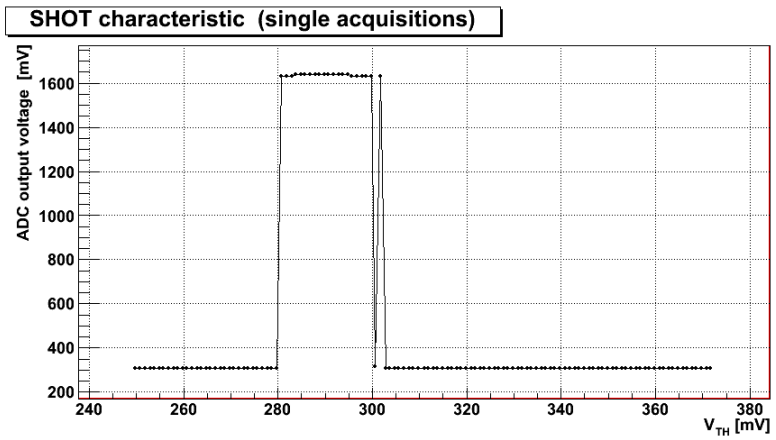

Figure 5.47: Threshold scan: SHOT characteristic.

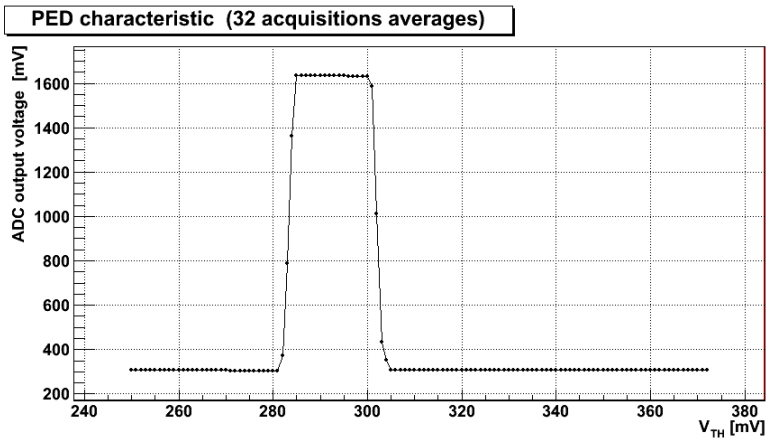

Figure 5.48: Threshold scan - PED characteristic.

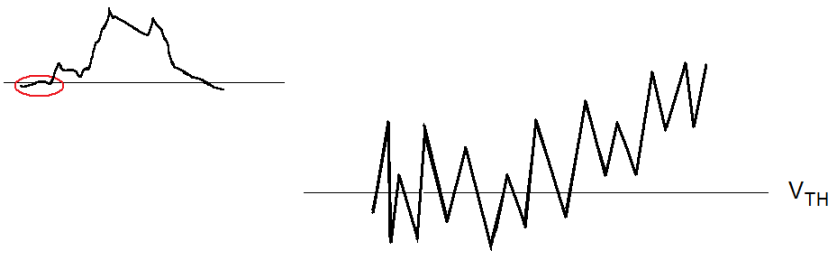

Figure 5.49: Thermal noise superimposed to the main parasitic signal, which leads to an indeterminate DFF output.

A more precise characterization can be performed with a fine threshold scan of rising and falling edges. In particular, for a few devices measurements have been obtained by varying V_{TH} with a step of 0.1 mV, in order to extract more than 10 points for each edge.
In Figure 5.50 and 5.51 are shown SHOT and PED characteristics for a representative device.
On the one hand, SHOT values are clearly indeterminate close to transition voltages. On the other hand, averages provided by PED acquisitions shape instead sharp rising and falling edges.

A measurement of the thermal noise voltage fluctuations has been obtained by fitting edges with two sigmoids [11]. Derivatives are Gaussian functions, hence the standard deviations quantify voltage fluctuations.
The rising edge fit prototype is provided by the Standard Normal cumulative distribution function,

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} dt\ e^{-t^2/2}$$

which is correlate with the error function $erf(x)$ through the relationship (see also [12])

$$\Phi(x) = \frac{1}{2}\left[1 + erf\left(\frac{x}{\sqrt{2}}\right)\right] \quad .$$

In particular, we obtain the right fit prototype by replacing x with $(x-\mu)/\sigma$, except for a normalization and a shift.
The falling edge fit prototype is provided instead by the complementary cumulative function $1 - \Phi(x) = \frac{1}{2}\left[1 - erf\left(\frac{x}{\sqrt{2}}\right)\right] = \frac{1}{2} erfc\left(\frac{x}{\sqrt{2}}\right)$.

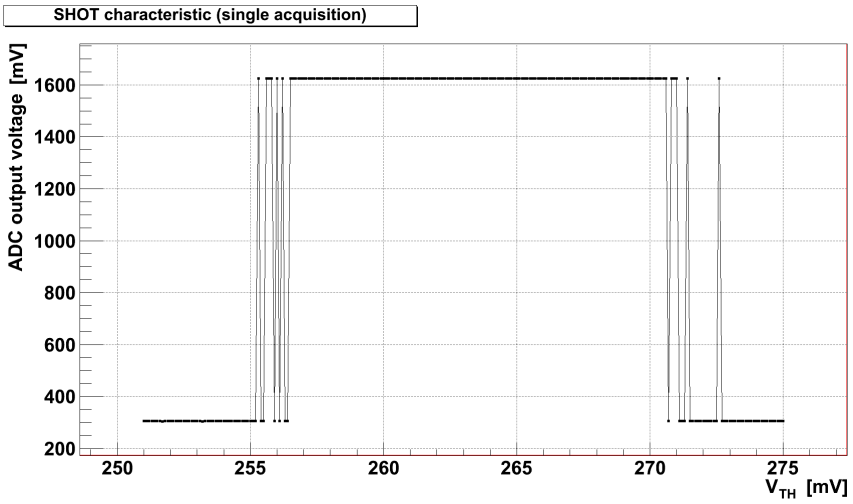

Figure 5.50: Fine threshold scan - SHOT characteristic.

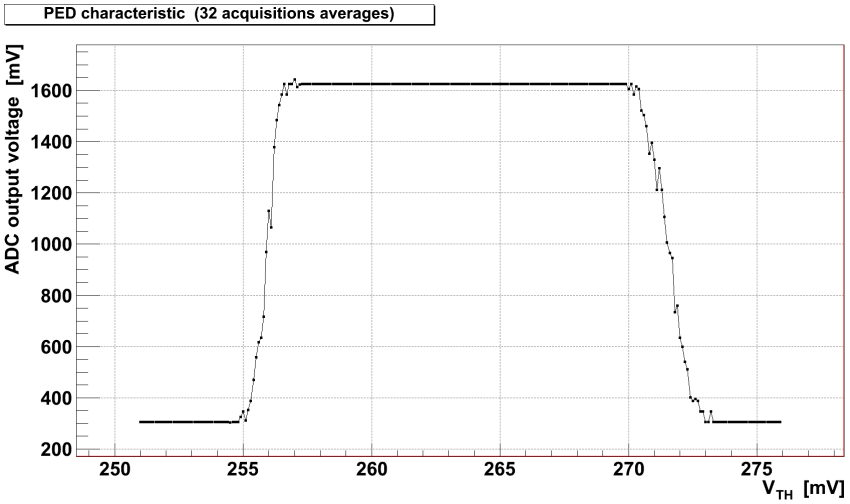

Figure 5.51: Fine threshold scan - PED characteristic.

Fits are shown in Figure 5.52, superimposing for each sigmoid its Gaussian distribution. Only for a better visualization, the normalizations are $1/\sqrt{2\pi}$ instead of $1/\sqrt{2\pi}\sigma$.
The standard deviations provided by fits are (0.38 ± 0.01) mV for the rising edge and (0.70 ± 0.01) mV for the falling one. Hence, thermal noise voltage fluctuations are negligible, below 1 mV.

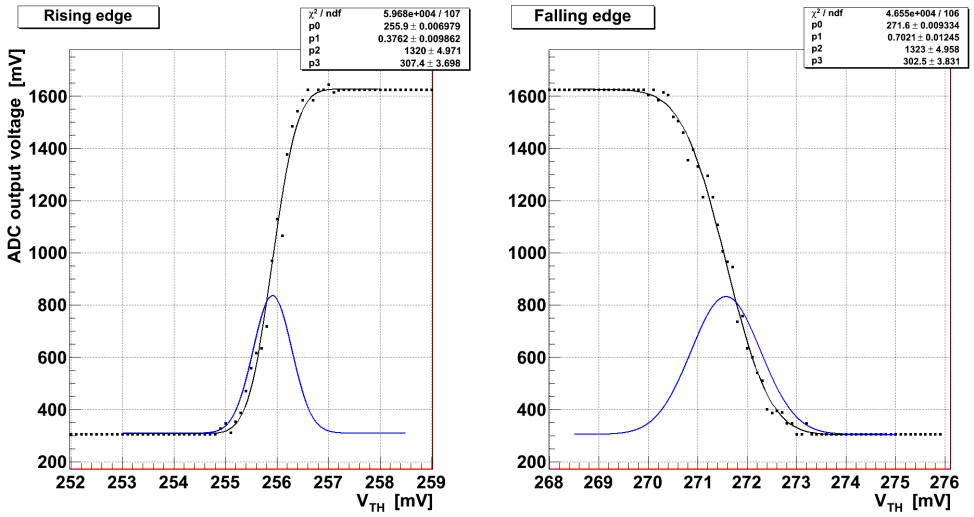

Figure 5.52: Rising and falling edges fits with sigmoids.

PREAMPs and DISCs homogeneity

The most significant test performed on matrix M3 is a characterization of the read-out electronics homogeneity. The first threshold scan shows that all DFF outputs become 1 but for different values of the threshold voltage V_{TH} within the 250 ÷ 370 mV range. Therefore PREAMPs and DISCs exhibit a certain *dishomogeneity*.
In particular, the set of 1024 PED characteristics shows both different edge transition voltages and plateau widths. For each characteristic two threshold voltages at the half-maximum rising and falling edges have been extracted. Moreover, the difference gives the full width at half maximum (FWHM) of the plateau, which is determinated by the noise amplitude.

The histogram shown in Figure 5.53 has been filled with rising-edge transition voltages. Reasonably, the spread of this distribution quantify the thresholds dishomogeneity. The standard deviation provided by the Gaussian fit is about 14 mV. This value is quite large if we take into account that a MIP should produce a signal of 38 mV for 30 μm of depletion layer and 10 fF of sensor capacitance, although the PREAMP stage then provides a nominal voltage gain of 12. Furthermore, simulations show that in order to allow the detection of a 600 electrons signal the nominal threshold is 220 mV (20 mV above the baseline). Thereby, a standard deviation of 14 mV for V_{TH} values becomes significant.
This result confirms difficulties introduced by the LePix aggressive and non standard layout. In particular, all PREAMPs and DISCs are integrated at the periphery of the matrix, requiring a very compact design necessary to meet the tight area requirements. This threshold dishomogeneity can be attributed to mismatches at the transistor level in DISC devices.

For the sake of completeness, Figure 5.54 shows the histogram of falling-edge threshold voltages. The Gaussian fit provides about the same previous standard deviation.

The histogram in Figure 5.55 has been filled instead with the FWHM of characteristics. The distribution shows a Gaussian trend followed by an excess of devices which have a much larger FWHM, between 18 ÷ 20 mV to 50 mV or beyond.
A certain Gaussian spread in the noise amplitude is expected. Reasonably, if the parasitic signal is injected before the PREAMP stage, it can be attributed to a dishomogeneity in the voltage gains .

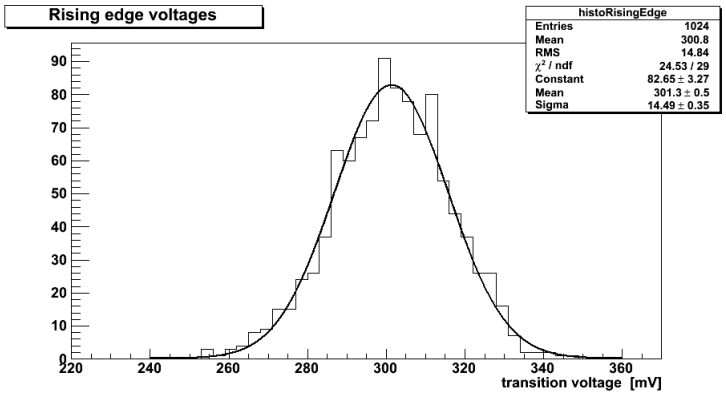

Figure 5.53: Rising-edge threshold voltages distribution.

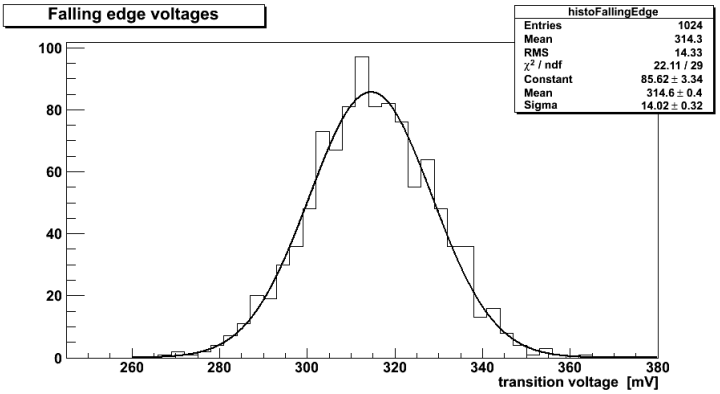

Figure 5.54: Falling-edge threshold voltages distribution.

However, the excess (about 10%) of devices with a much larger FWHM is somehow anomalous. Actually, no satisfactory explanation has been found for this result.
The first hypotesis has been to impute the excess to a systematic effect due to a coupling between analog and digital lines in the matrix. That is, a systematic noise injected into neighbouring analog lines from a digital path. In this case, some spacial clusterization of devices affected by a larger noise should be observed.
Nevertheless, as shown in Figure 5.56 reconstructing the exact position of each pixel in the matrix CORE part, there is no evidence of a systematic clusterization. DISCs which lead to a FWHM grater than 20 mV are scattered randomly.
Hence the actual cause remains something unknown. Perhaps, it just involves some faulty devices.

Before concluding, we have to note that of course in order to detect a particle hit or the test PULSE the threshold voltage V_{TH} must be higher with respect to the measured noise. However, as alreay mentioned no PULSE has been observed during tests.

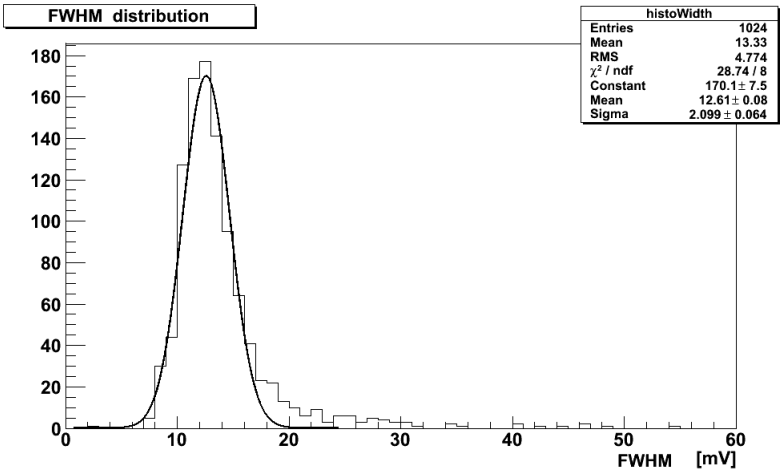

Figure 5.55: FWHM distribution.

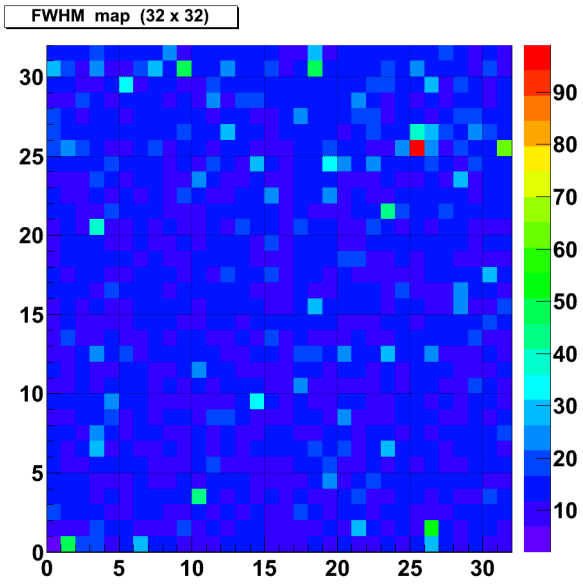

Figure 5.56: FWHM map (32 × 32).

Bias characteristics

All tests and measurements previously described have been performed using devices nominal bias conditions. Here we conclude the characterization of the matrix M3 describing PREAMP and DISC bias studies.
In order to better understand the procedure, a more detailed description of PREAMP and DISC internal structures is required.

A schematic of the voltage preamplifier is shown in Figure 5.57. The circuit is based on NMOS cascode input stage with PMOS cascode load. Cascodes ensure an acceptable DC gain and are coupled to gain-boosting auxiliary amplifiers. The output stage is a NMOS source follower, which ensures proper matching between DC levels in the internal nodes. The AC coupling is provided by the capacitor C_1 placed on the gate of the input transistor. Furthermore, a capacitive feedback is obtained with the second capacitor C_2. In order to optimize the proper impedance matching and to exploit the Miller effect, C_2 is connected between the gate of the input device and the gate of the output NMOS source follower. Hence the closed-loop voltage gain is determined by the ratio C_2/C_1, with a nominal value of 12. Both C_1 and C_2 have been implemented as metal-to-metal capacitors. Finally, a current feedback establishes the necessary DC path to bias the amplifier and to discharge the feedback capacitor after a signal has been detected. The feedback current source is implemented with a PMOS transistor which works in the saturation region when the output voltage rises of about 40 mV above the baseline.

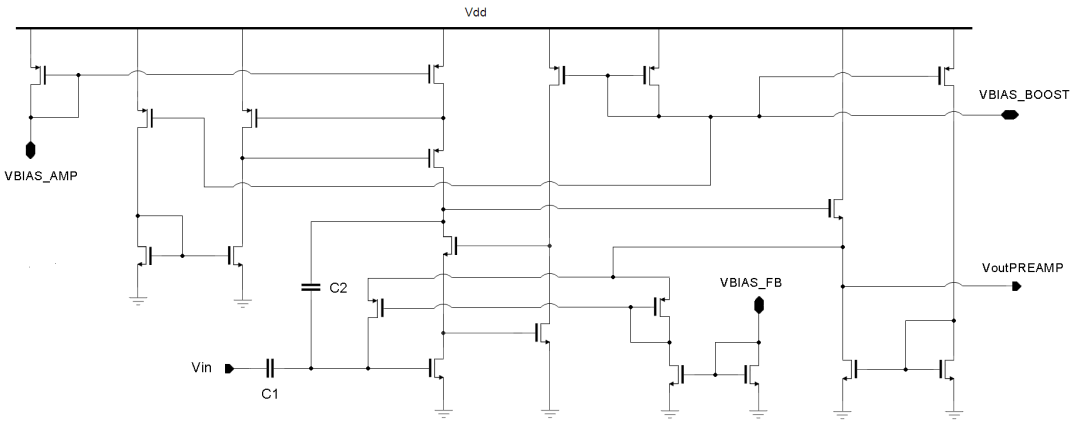

Figure 5.57: Schematic of the front-end voltage amplifier (PREAMP).

In perspective of measurements, we have to note that the amplifier has two independent bias currents that must be regulated externally. The pin VBIAS_AMP regulates the current in the main branch of the circuit with cascodes, whereas the pin VBIAS_BOOST allows the regulation of the bias currents flowing in the two gain-boosting transistors and in the NMOS output source follower.
Moreover, a third pin VBIAS_FB is used to regulate the feedback current, which determines the effective voltage gain of the circuit.

A schematic of the comparator is shown in Figure 5.58 instead. The circuit is based on a NMOS single-ended differential pair with PMOS active load, followed by two common source stages. At the end, the digital CMOS output pulse is generated by one inverter. The threshold voltage V_{TH} is fed to the negative input and the PREAMP output signal to the positive one. When the input signal is below the threshold the output voltage is zero. In contrast, when the input exceeds the threshold the output voltage flips to $V_{DD} = 1.2$ V, i.e. 1 in CMOS logic.
The bias current which flows into the differential pair is externally tunable through the pin VBIAS_DISC, whereas the bias currents of common source stages are fixed by current mirrors.

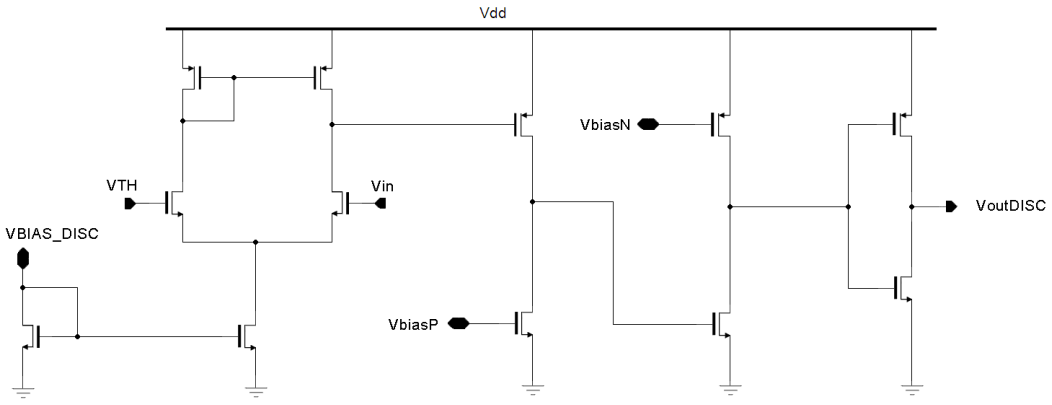

Figure 5.58: Schematic of the front-end comparator (DISC).

Each mentioned tunable bias current is independent, requiring a specific external circuit. Nevertheless, these currents are small, hence a simple voltage divider can be used to establish a reference voltage to which a fixed bias resistor is connected.
This allows to control bias currents by using simple trimmers, placed on the external test PCB.

For instance, in Figure 5.59 is shown the external circuit to bias the PREAMP input stage. Note that the transistor in the dashed area is located at the perifery of the matrix, while the trimmer and the other discrete components are placed on the test PCB. In particular, test points VBIAS_AMP and VBIAS_AMP_B can be directly probed with a multimeter. Hence, by varying the voltage at the trimmer output we can immediately know the bias current which flows in the 250 kΩ bias resistor. This current is identical to the one flowing in the main branch of the amplifier, being mirrored with an unitary aspect ratio by a PMOS current mirror.
Likewise, as shown in Figure 5.60, VBIAS_BOOST_B, VBIAS_FB_B and VBIAS_DISC_B trimmer-output voltages determine respective bias currents. From specifications, PREAMP internal currents are required in the 0.2 to 2 μA range and are generated using 250 kΩ bias resistors. The nominal PREAMP feedback current is between 2 and 10 nA. However, being mirrored with a 0.1 aspect ratio, a current in the 20 to 100 nA range flows through a 10 MΩ bias resistor. Furthermore, the DISC requires a current in the 0.25 to 1.5 μA range in the input differential pair, generated with another 250 kΩ bias resistor.

Experimental characteristics shown in Figure 5.61 have been obtained plotting the measured bias currents versus trimmer output voltages. Data are compared with theoretical values predicted by DC simulations.
The agreement between PREAMP characteristics and simulations is not satisfactory. However trends and currents ranges are reasonably close to simulations except for a systematic shift. A perfect agreement between data and simulated values has been obtained instead for the DISC characteristic. In particular, VBIAS_AMP_B and VBIAS_BOOST_B characteristics show a linear range followed by a saturation when the bias voltage exceeds 600 mV, while the feedback current characterisitic is linear on the whole VBIAS_FB_B range. The opposite behaviour occurs in the VBIAS_DISC_B characteristic. When the bias voltage is higher than 600 mV the trend is linear, whereas if the voltage is too low the current mirror which biases the differential pair of the DISC input stage is off, hence the bias current is correctly zero.
Of course, proper bias voltages must be choosen within the linear regions.

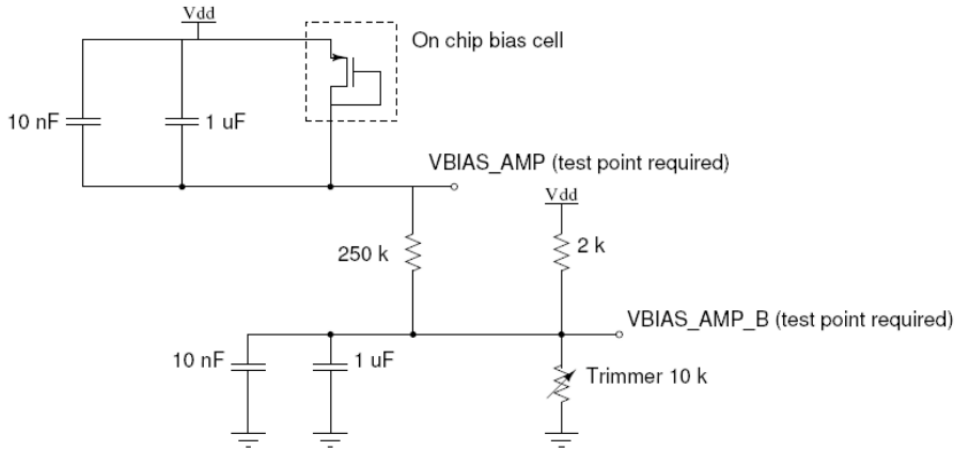

Figure 5.59: External circuit to bias the PREAMP input stage.

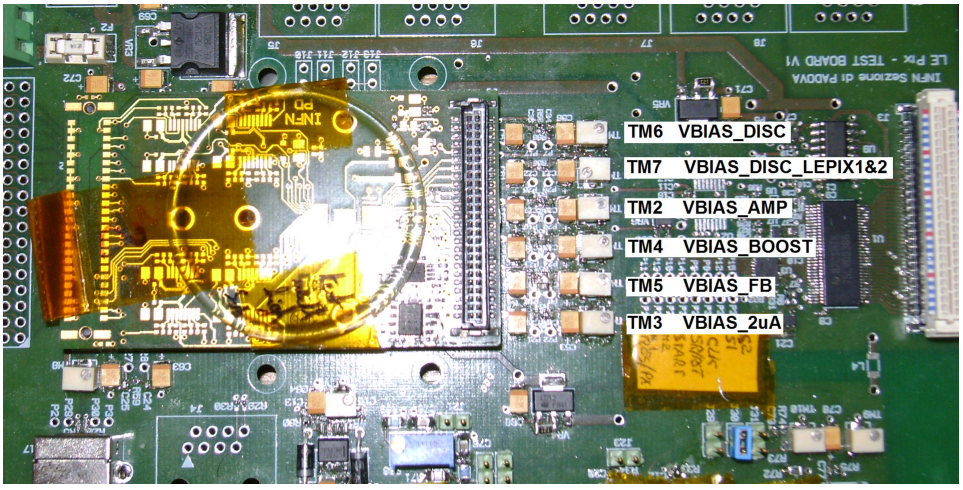

Figure 5.60: Test PCB external trimmers.

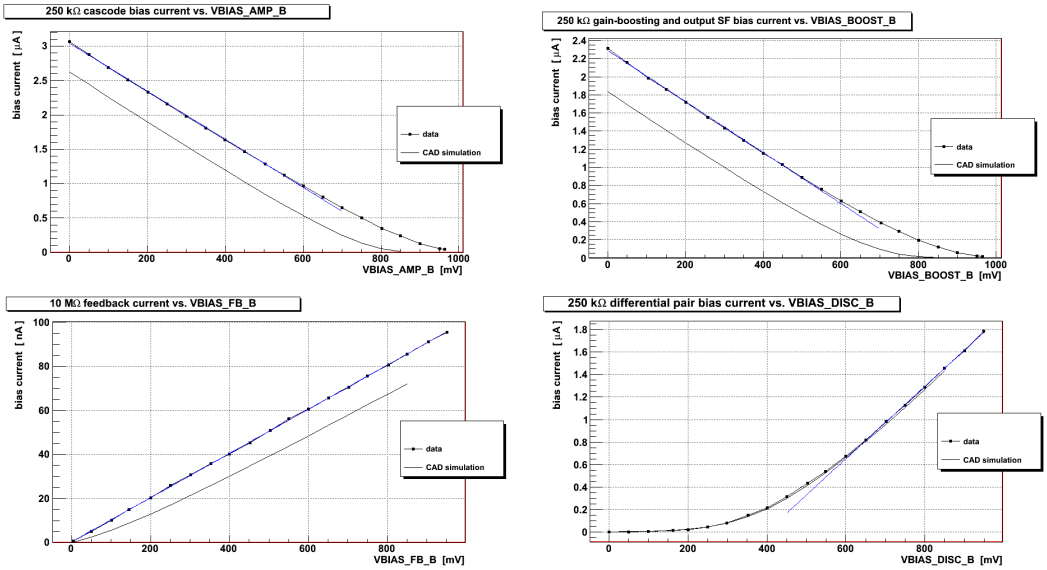

Figure 5.61: Experimental bias characteristics. Data are compared with theoretical values predicted by DC simulations.

Conclusions

The LePix project explores the possibility of implementing monolithic pixel detectors in very deep submicron CMOS technologies, offering a novel pixel architecture potentially suitable for the LHC upgrades and for future HEP experiments. At present both the ALICE and CMS collaborations have been shown an interest for the project.
According to the monolithic approach, the sensor and the front-end electronics are integrated on the same silicon wafer. The charge collection in the sensor is driven by drift, increasing speed and radiation tolerance. Furthermore, standard CMOS processes reduce the production cost.
Within the LePix collaboration, that at present involves CERN, INFN, IReS, Imperial College and C4i-MIND, INFN has been an important reference point.

This thesis has been devoted to the characterization of the matrix prototypes of the first LePix submission in standard 90 nm CMOS technology, exploiting the experimental setup available in the INFN laboratory in Turin since April 2011. The author has given his contribution both in the setup commissioning and in the implementation of the software for the off-line data analysis, providing tools to perform more systematic and faster matrix characterizations.

Pratical design and implementation of the LePix sensor layout are challenging, and the first submission with the foundry on standard resistivity wafers has shown that the exercise is not easy.
In particular, a layout problem arised during the first tests performed at CERN in summer 2010 and the lot on high resistivity wafers has been put on hold, requiring adequate corrections. This issue introduces severe limitations for the characterization of the detector, imposing the pixels exclusion.
Nevertheless, a systematic characterization of the read-out electronics performed in Turin has validated the embedded circuitry implemented in first matrix prototypes.

Tests results have demonstrated a good homogeneity of the source followers employed in the first read-out architecture, which involves a MAPS-like serial read-out. On the other hand, the second front-end scheme, based on a binary serial read-out with a voltage preamplifier followed by a comparator, has shown a certain dishomogeneity, due to the non standard and aggressive layout necessary to meet the tight area requirements.

After corrections, test structures on high resistivity substrates have been submitted and they are expected back from the foundry in October 2011. Tests performed on these prototypes will define the actual LePix capabilities.

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