EXPERIMENT #10

CMOS OP AMPS

I OBJECTIVES

The objective of this Experiment is twofold: to provide insights into the structure of basic two-stage CMOS amplifiers, and to provide experience with larger-systems applications using a relatively large number of CMOS device arrays.

II COMPONENTS AND INSTRUMENTATION

The primary requirement is for three CD4007 CMOS array ICs. Up to four additional CD4007 can be used for optional enrichment explorations. As well, you need a good collection of capacitors ranging from 10 pF to 0.1μF in a 0.1, 0.33 sequence, a low-inductance low-leakage (ceramic) capacitor of at least 1μF as well as power-supply bypass capacitors. As for equipment, you need a dual power supply, DMM, waveform generator and dual-channel oscilloscope. As well, a capacitor box having 4 or more decades would be useful, though not essential. For convenience, Fig. 10.1 prdvides various views of the CD4007 package.

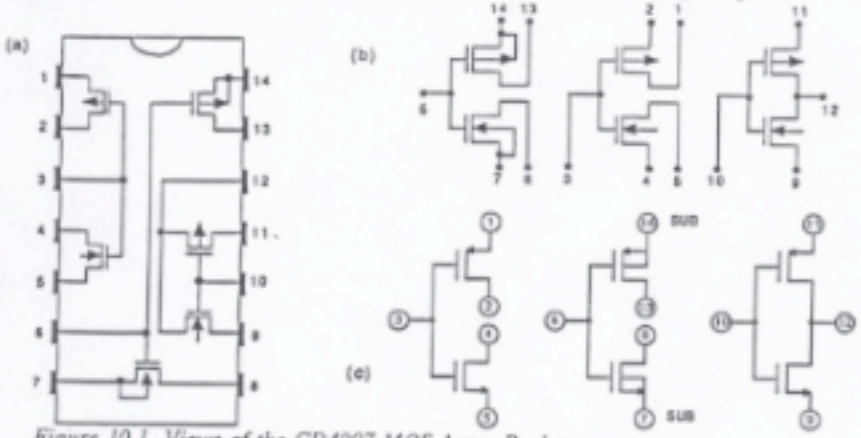

Figure 10.1 Views of the CD4007 MOS Array Package

III READING

Concentration will be on Sections 10.7 and 10.8 of the Text. Familiarity with MOS devices and particularly part of Section 5.7 on CMOS is assumed. Reference will also be made to material on pulse circuits in the latter part of Appendix F of the Text, and to aspects of feedback including resistance modification in Section 8.2, and pole splitting in Section 8.11.

IV PREPARATION

Following the usual pattern in this Manual, **Preparation** tasks are keyed directly to the **Explorations** to follow, by the use of the same titling and section numbering, augmented by the prefix P. Note that there are a large number of preparations here, some of considerable complexity. Clearly, not all can be quickly done. But neither can all of the Explorations! The challenge for you here is to select some of the suggested preparatory investigations to work on. They are very informative, but also time consuming.

• THE BASIC AMPLIFIER

P1.1 DC Operation

(a) Consider the CMOS amplifier in Fig. 10.2 employing transistors for which $|V_t| = 1V$, $k = 0.50$ mA/V, and $\lambda = 1/50V$. For ± 7.5 V supplies, $R_1 = 220k\Omega$, $V_F = V_B$, and $V_A = 0V$, estimate all node voltages and device currents, assuming the effect of λ to be negligible.

(b) Now, estimate r_o for each device and the change in bias current that implies.

(c) What difference in the value of V_t for Q_{1B} and Q_{2B} would account for a measured offset of 30mV?

(d) For the bias situation identified in (a) above, find g_m for each device.

(e) Using the value of r_o estimated in (b) and of g_m in (d), estimate the open-loop gain of the amplifier v_o/v_{id}.

• AC UNITY-GAIN OPERATION

P2.1 Over-Compensated Operation with a Dominant Load Pole

(a) Consider the circuit of Fig. 10.2 in which $R_2 = \infty$, $C_2 = 0$ and for which nodes F and B are joined, with a load capacitance, $C_1 = 0.1\mu F$, connected from node F to ground. Estimate its output slew rate for large positive-going and negative-going inputs for which one of Q_{1B} or Q_{2B} is cut off. Also find an approximation to the corresponding 10% to 90% rise and fall times.

(b) Using the values of open-loop output resistance and gain identified in P1.1 (b) and (e), with the relevant value of feedback β, estimate (roughly) the gain and output resistance of the closed loop.

(c) What "high-frequency" 3dB frequency to you expect?

P2.2 Minimal Load-Capacitance Compensation

(a) Consider the circuit of Fig. 10.2 as an open-loop amplifier with a load capacitance $C_1 = 0.1\mu F$. Assume that the amplifier's dynamics are controlled by the output pole and the Miller-Effect-influenced pole at the gate of Q_{6C}, whose C_{gd} is perhaps 2pF, and for which wiring capacitance at node E is possibly 15pF. Estimate the two poles.

(b) Prepare a corresponding Bode magnitude plot of open-loop gain, on which a line for $\beta = 1$ is included. Comment on the stability of the corresponding closed loop.

P2.3 Internal Compensation

(a) Consider the situation in which the output capacitor at node F of Fig. 10.2 is reduced to 100pF, for the conditions in which, for Q_{6C}, $C_{gd} = 2pF$, and C_{stray} (due to wiring) at the gate and drain are perhaps 15pF each. Using Eq. 10.49 and 10.50 of the Text, estimate the location of the corresponding poles.

(b) Prepare a corresponding Bode magnitude plot on which a line for $\beta = 1$ is included. Comment on stability.

(c) For the situation investigated above, to what frequency must the lower pole be moved to ensure stability with 45° phase margin? with 65° phase margin?

• HIGHER-GAIN OPERATION

P3.1 An Amplifier with Gain of +100 V/V

(a) For the amplifier of Fig. 10.2 as analyzed in the Preparations above, embedded in the 100 kΩ-10kΩ loop described in E3.1, what closed-loop gain results?

P3.2 Open-Loop Gain

(a) Sketch the circuit described in E3.2, using a triangular amplifier symbol. Calculate the open-loop gain of the amplifier as detailed earlier, which applies at very-low and relatively-high frequencies.

(b) On a Bode magnitude plot of open-loop gain, using the low-frequency value found in (a), with poles as estimated in P2.3 (a) {admittedly with a small load capacitor, a fact we will ignore here}, plot a $1/\beta$ line corresponding to the 10MΩ, 1μF feedback network. Comment on stability. What about the situation with a load resistor of 100kΩ?

• EFFECTS OF DEVICE SIZING

P4.1 Many Possibilities

(a) For one or more of the revised circuits (a), (b), (c) (or any combination) alluded to in E4.1, find the corresponding bias currents and open-loop gain, using the conditions presented in P1.1 (a) above, and ignoring the effects associated with λ.

V EXPLORATION

• THE BASIC AMPLIFIER

The basic amplifier on which you will experiment resembles the two-stage topology shown in Fig. 10.23 of the TEXT. This is depicted here as well, in Fig. 10.2. Note a major difference here is that choice of device ratios is limited by virtue of array device matching. Initially, the amplifier will be stabilized for low-frequency operation by a large load capacitor.

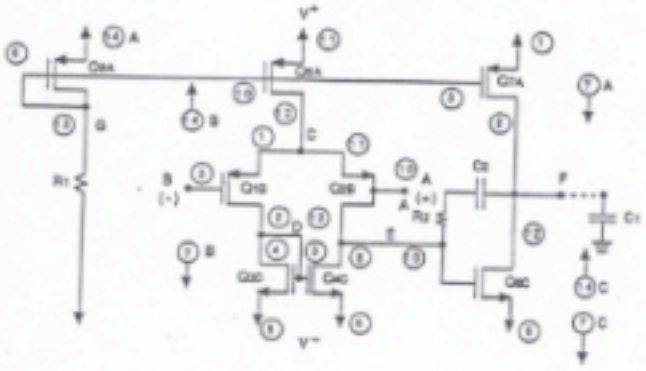

Figure 10.2 A Basic Two-Stage CMOS Op Amp. Three CD4007 arrays (A, B, C) are required. Pin numbers are for the corresponding package. Note the 6 substrate connections, which are essential for correct operation of the arrays

E1.1 DC Operation

• **Goal:**

To verify the DC operation of the assembled CMOS op amp.

• **Setup:**

○ Assemble the circuit shown in Fig. 10.2 using ± 7.5 V supplies, $R_1 = 220\text{k}\Omega$, $R_2 = \infty$, and $C_2 = 0$ pF. Connect the positive input (A) to ground, the negative input (B) to the output (F), and a capacitor $C_1 = 0.1\mu\text{F}$ from output (F) to ground.

• **Measurement:**

a) With zero input voltage, verify that the amplifier is stable by measuring first node F and then node E with your oscilloscope, using a ×10 probe.

b) Using your DVM with a series 10 kΩ resistor as a probe (to minimize various effects of the meter leads), measure (some of the) dc voltages at nodes A through G.

• **Tabulation:**

V_A, V_B, V_C, V_D, V_E, V_F, V_G.

• **Analysis:**

Consider the offset voltage you have found. Over what range of input voltages would you expect the output to follow the input reasonably well?

E1.2 Evaluating the Linear Operating Range

• **Goal:**

To investigate the range of (linear) operation of the amplifier as bias current changes.

• **Setup:**

○ Connect the positive input (A) to the center-tap of a 10 kΩ potentiometer (R_3) whose ends are connected to the positive and negative supplies. The negative input (B) remains connected to the output (F).

• **Measurement:**

a) While measuring the offset voltage directly (between nodes A and B), with your DVM, use R_3 to raise and lower the voltage on node A. For the two settings of pot R_3 at which the offset changes by 0.1 V from its mid-level value, measure the voltages at nodes A, B (and others as you see fit).

b) Repeat the previous step with R_1 shunted by a resistor, R_4, of equal value. In particular, note the offset voltage for $V_A = 0$, and the voltages at nodes A through G at which the offset changes by 0.1 V, and by 0.2 V.

• **Tabulation:**

R_1, V_{AB}, V_A, V_B, and others, for interesting values of V_A using two offset thresholds.

• **Analysis:**

Consider the fact that the change in offset voltage at the extremes of input voltage represents the edge of linear operation for large input signals. Try to identify the part of the circuit at which the critical nonlinearity occurs.

• AC UNITY-GAIN OPERATION

E2.1 Over-Compensated Operation with a Dominant Load Pole

• **Goal:**

To explore the amplifier's operating dynamics.

• **Setup:**

○ Assemble the circuit of Fig. 10.2 as indicated in Exploration E1.1 above, but with input A connected to a waveform generator (node I), via a resistor, $R_5 = 10$ kΩ.

• **Measurement:**

a) Using your (normalized) dual-channel oscilloscope, and a 4 Vpp input square wave at 100 Hz, compare the waveforms at A and F. What are the relative amplitudes? What are the times taken for 50% of the total output change? for a change from 10% to 90% of the final output? Sketch the waveforms at A and F.

b) With input A shunted to ground with a 100Ω resistor, repeat the previous measurements [with an input signal about 1% as large as before].

c) With conditions otherwise the same as in step b), change the generator input to a sine wave and measure the voltage gain by comparing peak-to-peak values. Now, raise the input frequency until the gain is 0.707 of its lower-frequency value (that is, until it has dropped by 3dB).

• **Tabulation:**

v_A, v_F, t_{50}, t_{90}, v_o, v_f, f.

• **Analysis:**

Consider the operation of the circuit as a follower, including estimates of its gain, slew rate, and large- and small-signal bandwidths. Use the relationships in Appendix E of the Text, in particular equation (E.13), to relate rise-times and bandwidths.

E2.2 Minimal Load-Capacitance Compensation

• **Goal:**

To explore the effects of moving to more minimal compensation.

• **Setup:**

○ Use the circuit of Fig. 10.2 as connected in steps b) and c) of Exploration E2.1 above. As well, in preparation for the next step, shunt the load capacitor, C_1 = 0.1μF, by a second capacitor, C_{10} = 100pF, wired with very short leads from output F to ground.

• **Measurement:**

a) With a 4Vpp square wave at 100Hz applied at the input, note the output waveform in some detail, particularly at the times following slewing where linear operation begins (and continues).

b) Replace C_1 by a capacitor decade box set to 0.1μF. Again observe the output. For a reasonable box and relatively short connections, you can expect the waveforms to be quite similar to those found previously. If not, you will have to use a selection of discrete capacitors in what follows.

c) With a 0.1Vpp square wave at 100 Hz at node A, and ×10 probes at nodes A, F, reduce the primary load capacitance C_1 until a peaked oscillatory response is seen at F. Choose a value of C_1 for which the overshoot is some reasonable value (say 10 to 20%). Note the value of C_1 (including the small capacitor C_{10}). Call it C_{12}. (To be somewhat consistent, let C_{11} = 0.1μF be the original value of C_1.)

• **Tabulation:**

Overshoot, C_{12}.

• **Analysis:**

Consider the possible improvement in dynamics you can expect. By what factor will the slew rate change?

E2.3 Internal Compensation

• **Goal:**

To explore the possibility of internal-feedback compensation.

• **Setup:**

○ Use the test setup as established in the last step of E2.2. With C_{12} connected as a combination of discrete capacitors, install R_2 and C_2 as shown in the circuit of Fig. 10.2. Select R_2 initially large (say R_{20} = 100 kΩ), with C_2 initially small (say C_{20} = 10 pF).

• **Measurement:**

a) Display nodes A and F using 10× probes. Increase C_2 from C_{20} to C_{21}, a value at which the overshoot at F reduces by 20 to 30% or so from the value established in the last step of E2.2.

b) With $C_1 = C_{12}$ and $C_2 = C_{21}$, reduce R_2 (by shunting) from R_{20} until the overshoot is minimized, at $R_2 = R_{21}$.

c) With $C_1 = C_{12}$, $C_2 = C_{21}$ and $R_2 = R_{21}$ initially, change C_1 from C_{12} to C_{13} for which the overshoot is again as large as it was at the end of the last step of E2.2.

d) Change C_2 from C_{21} to C_{22} in an attempt to reduce the overshoot once more. Then, change R_2 to R_{22} and C_2 again, iteratively, to reduce the overshoot. Call the values finally chosen C_{13}, C_{23} and R_{23}, for convenience.

e) Now, if time permits, evaluate the effect of changing C_1 from C_{13}, particularly as it is increased.

f) Now, with the input changed to a 0.1Vpp sine wave, initially at 100 Hz, raise the frequency until the gain falls to 0.707 of its low-frequency value, noting any voltage peaks along the way.

• **Tabulation:**

C_1, C_2, R_2, overshoot, in many combinations leading ideally to small C_1 and small overshoot.

• **Analysis:**

Consider the virtues and deficiencies of the unity-gain stabilization process you have just gone through.

• HIGHER-GAIN OPERATION

E3.1 An Amplifier with a Nominal Gain of +100

• **Goal:**

To evaluate operation at increased gain.

• **Setup:**

○ Connect the circuit of Fig. 10.2 with ± 7.5 V supplies, R_1 = 220kΩ, $R_2 = R_{21}$ = 100 kΩ, $C_2 = C_{23}$, and load capacitance $C_1 = C_{23}$, or $C_1 = C_2$ = 100pF, if in doubt. Externally, connect a feedback network from node F to node B consisting of a 100kΩ feedback

resistor and 1 kΩ to ground, with a 100kΩ, 1kΩ input-signal divider (with the 1kΩ grounded) connected to the positive amplifier input (A) from the generator (I).

• **Measurement:**

a) Adjust a square-wave input at 100Hz to provide an output of 1V pp. Measure the peak-to-peak voltage at nodes F and A in order to estimate the closed-loop gain.

b) Note the output overshoot. Remove the load capacitor (C_1), and note the overshoot again.

• **Tabulation:**

C_1, v_A, v_F, overshoot.

• **Analysis:**

Consider your estimate of the closed-loop gain. Note, as we shall verify shortly, that its value is affected by the resistance level of the feedback network. Note also that the loop is more easily stabilized for nominal gains >>1. What evidence do you have for this?

E3.2 Open-loop Gain

• **Goal:**

To measure the open-loop gain by introducing external dominant-pole compensation.

• **Setup:**

○ Connect the circuit of Fig. 10.2 as described in E3.1 setup, with an input attenuator as indicated, but with a feedback network consisting of a 10MΩ resistor R_f from output F to the negative input B, and a large low-leakage capacitor (C_3 = 10 μF, tantalum) from B to ground. Use a sinewave input initially at 10 kHz.

• **Measurement:**

a) Adjust the input for an output of 1 V pp at F.

b) Vary the frequency, and note the upper and lower 3dB frequencies.

c) Assuming a midband region of at least a frequency decade, measure the midband gain. (If the midband is seen to be very narrow, R_f or C_3 must be increased.)

d) Repeat all of the previous three steps with a resistor R_L = 1MΩ connected from the output directly to ground. (If the output offset is large, use a capacitor of 0.1μF in series with R_L.)

e) Repeat the entire three-step process again with R_L = 100kΩ.

• **Tabulation:**

R_L, v_o, v_f, f_H, f_L with $R_L = \infty$, 1 MΩ and 100 kΩ.

• **Analysis:**

Consider the open-loop gain you have found, and its dependence on load resistance. Consider also the dependence of the low-frequency cutoff on the value of R_L as it affects the resistance seen by C_3 [See section 8.2 of the Text].

• EFFECTS OF DEVICE SIZING

E4.1 Many Possibilities

While there is limited flexibility available in the control of device sizes when using arrays, one possibility exists. In general, it is to directly parallel array components. The primary precaution to take is to ensure that both the p-channel and n-channel substrates are appropriately connected (to the +ve and –ve supplies respectively).

Several interesting possibilities for parallel connection exist:

(a) Paralleling Q_{1B} and Q_{2B}, with components from a fourth array;

(b) Paralleling Q_{3C} and Q_{4C}, with components from a fifth array;

(c) Paralleling Q_{7A} and Q_{8C}, with components from 2 additional arrays (arrays numbered 4, 5 (or 6, 7 if 4, 5 are already employed in a), b))).

While essentially any of the preceding Explorations can be repeated with such changes, those in E1.1 and E3.2 are quite informative. Obviously, there are a great many possibilities!

CMOS Op-Amps are increasingly important in analog signal-processing systems implemented in Very Large Scale Integration (VLSI).