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NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber ☆

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Abstract

For the full exploitation of the excellent timing properties of the Multigap Resistive Plate Chamber (MRPC), front-end electronics with special characteristics are needed. These are (a) differential input, to profit from the differential signal from the MRPC (b) a fast amplifier with less than 1 ns peaking time and (c) input charge measurement by Time-Over-Threshold for slewing correction. An 8-channel amplifier and discriminator chip has been developed to match these requirements. This is the NINO ASIC, fabricated with 0.25 μm CMOS technology. The power requirement at 40 mW/channel is low. Results on the performance of the MRPCs using the NINO ASIC are presented. Typical time resolution σ of the MRPC system is in the 50 ps range, with an efficiency of 99.9%.

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Keywords: Resistive plate chambers; ALICE; Time-of-flight; Fast amplifier; Discriminator; ASIC; CMOS technology

1. Introduction

The Time-of-Flight array for the ALICE experiment will be built using Multigap Resistive Plate Chambers (MRPC) in the form of strips, each with an active area of 1.2 m × 7.4 cm, read out with 96 readout pads of 2.5 × 3.7 cm^2 area [1].

☆ Developed by the LAA Project, CERN.

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Since exceptional time precision is needed, small gas gaps (250 μm width) are employed; to reach maximum efficiency 10 gas gaps are used, arranged in a double stack as shown schematically in Fig. 1. It should be noted that with this design each cell has a single anode readout pad and two identical cathode readout pads. Since the coupling between the movement of charge in any of the 10 gas gaps to the pickup electrodes is the same, the induced signal will be the sum of the signals from the gas avalanches occuring in any of the gaps. Due to the narrow gap, the induced signal will be produced 500 ps after the passage of the through-going charged particle and have a rise time of some hundreds of picoseconds.

The reason for building the detector as a strip is two-fold. One reason is that the strips can be tilted so that the detector plane is normal to incoming particles in the $r\theta$ plane; therefore the surface of the pickup pad is a plane at a fixed distance from the interaction point (thus the time of arrival does not depend on the impact point). The other reason is that it allows the readout of both anode and cathode pad, thus deriving a differential signal from the detector. Initially we had tried building a planar device reading out anode pads on one side with the return path to the cathode pads through the metallic box of the detector. This scheme introduced extra noise that caused degradation of the time resolution [2].

Early on in our development we found that the MAXIM 3760, a transimpedance preamplifier for 622 Mbps ATM applications, operated well as a front-end amplifier. This was coupled to an ECL discriminator (MAXIM 9691). An analogue signal was derived from this circuit, the charge of which

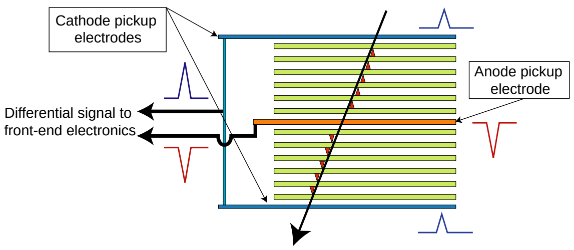

Fig. 1. Schematic representation of a 10 gap MRPC. The produced signal is differential.

was measured by an ADC and used for off-line slewing correction. However, for ALICE the time of hits in the TOF array will be digitised with an ASIC known as the HPTDC [3], with 25 ps bins and that can measure both the leading and trailing edge of the input signal. Thus, the front-end electronics should encode the charge of the input signal into the width of the output signal (time-over-threshold). One obvious problem of the MAXIM solution is the power used, 300 mW. In addition, these amplifiers and discriminators come in discrete packages and thus the front-end card has to be relatively large. It is clear that a low power, ultra-fast front-end ASIC is an important improvement for the front-end of the ALICE TOF.

2. Design of the NINO ASIC

The NINO ASIC had to satisfy the following requirements: (a) differential input; (b) optimised to operate with 30 pF input capacitance; (c) LVDS output; (d) output pulse width dependent on the charge of the input signal (need not be a linear dependence); (e) fast amplifier to minimise time jitter, i.e. first stage with a peaking time of ~ 1 ns; (f) threshold of discriminator adjustable in the range 10–100 fC; (g) eight channels per ASIC. The design of the circuit was outsourced.[1] The layout was done at CERN and submitted as part of a MPW run to IBM (0.25 μm CMOS).

The circuit has been previously discussed [4]. The detector is connected to the input of the NINO ASIC with a short transmission line; thus the input impedance has to match the transmission line and an open loop current to voltage conversion (no feedback) should be used. The circuit as shown in Fig. 2 satisfies these requirements. The input current pulse is fed into the source of the NMOS (M1) transistor, emerges from the drain and is again fed into the source of the second NMOS (M2) transistor. The current pulse will then emerge from the drain of M2, but the impedance at this point is very different (much larger) than at the input. This current charges the

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capacitance (which is the unavoidable stray capacitance associated with the transistor) on the drain; the rise time of this signal is governed by the characteristics of the transistor itself while the fall time is given by the time the capacitance C takes to be recharged (i.e. RC). The input impedance is $(1/g_{\mathrm{m}})_{\mathrm{M1}}$ and therefore the biasing and geometry of M1 is chosen to keep this impedance low to match the transmission line carrying the input signal. The output voltage is defined by the parasitic capacitance C and thus M2 is designed to minimise this capacitance.

A block diagram of the NINO (version 2) is shown in Fig. 3. The input stage is followed by 4 stages of low-gain, high-bandwidth differential amplifier. A slow feedback circuit supplies current to ensure that the input stages remain correctly biased. In addition an offset is added at this point that acts as a threshold adjustment. There is a stretcher just before the LVDS output driver. The pulse width before stretching varies between 2 ns and 7 ns; the HPTDC [3] that will be used in ALICE can only measure both leading and trailing edges of an input pulse for widths greater than 6 ns; thus the pulse stretcher will increase the pulse width by 10 ns.

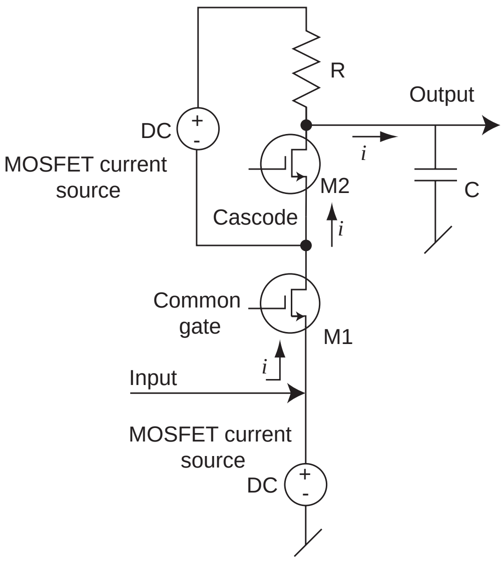

Fig. 2. Schematic input stage of the NINO ASIC.

3. Performance

The performance of the NINO ASIC attached to the MRPC strip was tested at the CERN T10 beam using 6 GeV/c pions. The time t0 of the incoming pion was measured by two scintillator bars read out with 4 Hammamatsu photomultipliers. The time jitter of t0 was 30 ps and was subtracted in quadrature from the measurements of the time resolution of the device under test.

The output of the MAXIM FEA card was ECL pulse for the leading edge and an analogue signal that was measured with a CAMAC ADC (LRS 2249W).

The time of the leading edge has to be corrected for the amplitude of the signal. Thus, this correction was made using the ADC value in the case of the MAXIM FEA and using the time width for the NINO FEA. The time width of the output pulse from the NINO ASIC varies rapidly for

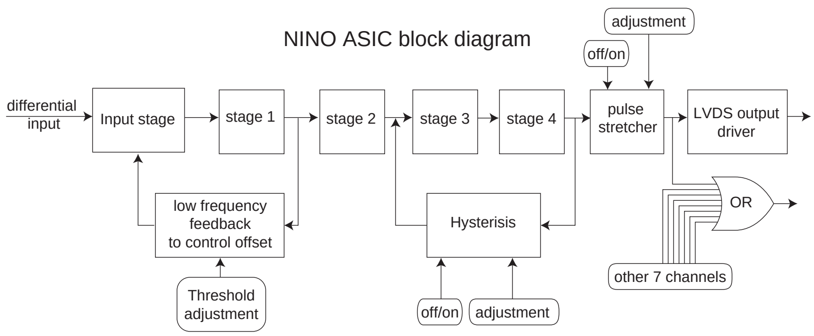

Fig. 3. Block diagram of the NINO ASIC.

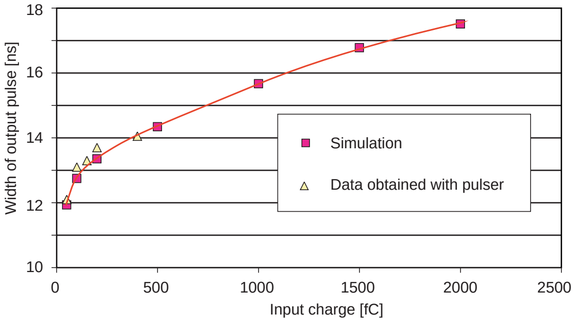

Fig. 4. Width of output pulse as a function of input charge. The expected behaviour from the simulation of the NINO ASIC is also shown.

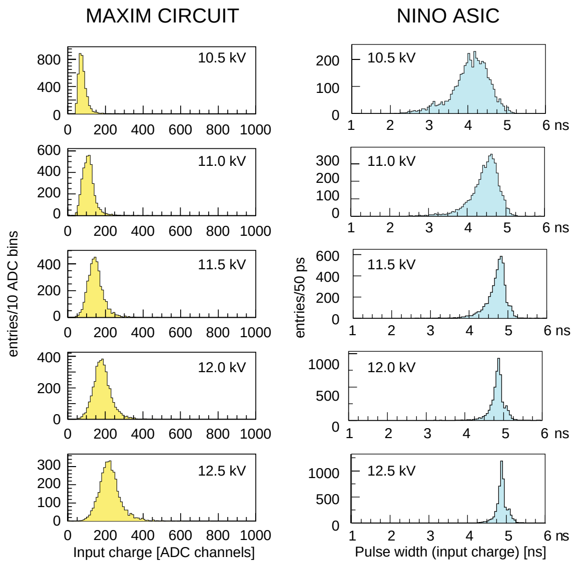

Fig. 5. Distributions of the signal charge. The left-hand spectra are obtained with the MAXIM 3760 circuit coupled to an ADC. The right-hand spectra show the time-over-threshold produced by the NINO ASIC.

small pulses and has a smaller variation for larger signals. This is shown in Fig. 4. Since time slewing is more evident for signals close to the threshold, this non-linear behaviour is a desired effect. We show in Fig. 5 the distributions of the measured charge. The left-hand plots are for the MAXIM 3760 circuit coupled to an ADC while the right-hand plots are the time-over-threshold (TOT) measurement made for the NINO ASIC. Note that the dynamic range increases for small input charge for the NINO ASIC TOT measurement.

In Fig. 6 we show a scatter plot of the time of the hit versus ADC value (for the MAXIM 3760 case) and versus TOT for the NINO ASIC. This is shown for 10.5 kV applied voltage.

We show in Fig. 7 the efficiency and time resolution. Both measurements were done with 60 fC threshold (measured using a pulser). The increased sensitivity exhibited by the NINO ASIC

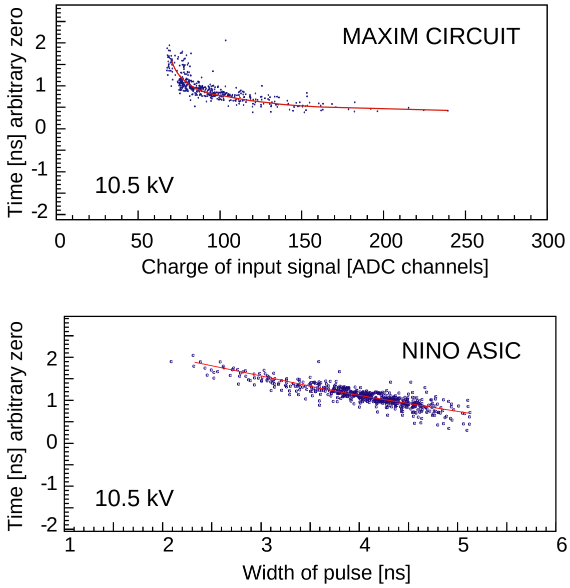

Fig. 6. Scatter plot of measured time versus charge.

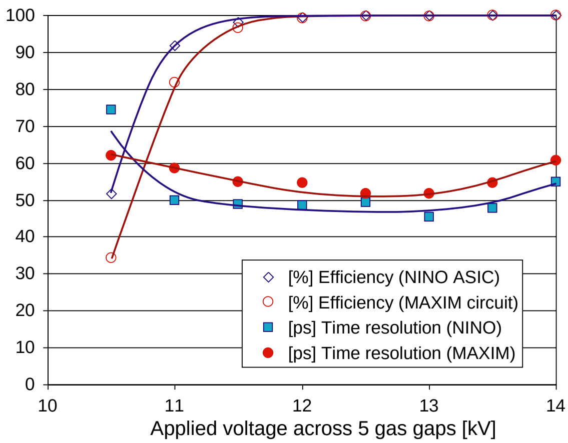

Fig. 7. Efficiency and time resolution using the MAXIM circuit and the NINO ASIC.

we believe is due to the differential input. Thus, with the NINO ASIC the MRPC strips can be operated at 500 V lower applied voltage; this makes the streamer-free range of the efficiency plateau even larger.

4. Summary

The NINO ASIC was purposely designed as the front-end amplifier/discriminator for the MRPCs used for the TOF array of the ALICE experiment. There are important advantages of the NINO ASIC compared to our baseline solution, a circuit based on the MAXIM 3760. The power consumption is a factor 10 lower (40 mW/channel). The output pulse, after time stretching, matches the width requirements of the HPTDC foreseen for the readout. Thus, the signal charge is measured by time-over-threshold (the time of the leading and trailing edge of the pulse). The circuit has differential input and is differential throughout. This leads to increased sensitivity and increased immunity to cross-talk.

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