RX64DTH —A Fully Integrated 64-Channel ASIC for a Digital X-ray Imaging System With Energy Window Selection

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***Abstract*—We report on the multichannel IC (RX64DTH) designed for position sensitive X-ray measurements with silicon strip detectors and dedicated to medical imaging applications. This integrated circuit has a binary readout architecture with a double threshold allowing on selection energy window for measured signals. The design was realized in a 0.8 μm CMOS process. The core of the RX64DTH IC consists of 64 readout channels. The single channel is built with four basic blocks: charge sensitive preamplifier, shaper, two independent discriminators, and two independent 20-bit counters. Each readout channel counts pulses which are above the low discriminator threshold and counts pulses independently above the high discriminator threshold. The energy resolution in such architecture is limited by the noise of a single channel and by channel to channel threshold spread. We present the noise and matching performance of a 384-channel module built with a silicon strip detector and six RX64DTH ICs. In the 384-channel module an equivalent noise charge of about 200 el. rms is achieved for the shaper peaking time of 0.8 μs and strip capacitance of 3 pF. The deviation of discriminator thresholds for the whole system is only 87 el. rms. The obtained results show that the energy resolution and uniformity of analog parameters (noise, gain, offset) are sufficient for medical diagnostic applications such as dual energy mammography and angiography.**

***Index Terms*—ASIC, digital X-ray imaging, front-end electronics.**

I. Introduction

DIGITAL X-ray imaging systems consisting of multi-element sensors and multichannel readout ASICs are very promising alternatives to traditional medical imaging systems due to their post-processing capability, large dynamic range, good spatial resolution and high count rate capability. If additionally such digital imaging systems are able to extract some energy information about X-ray radiation, it would be very advantageous, especially in medical radiology (contrast improvement, dose reduction) [1]–[5].

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In building an X-ray imaging system the first questions to be answered concern the type of detector used and readout electronics. We propose to use a silicon strip detector (SSD) in edge-on configuration [5] together with the 64-channel ASIC called RX64DTH (DTH—Double Threshold) with a binary readout architecture and with the possibility of an energy window selection of input signals for each readout channel. Using six RX64DTH ICs and the SSD we have built a 384-channel position sensitive module. It has been characterized for noise and matching performance having in mind possible future applications like dual energy mammography and angiography.

The paper is organized as follows. In Section II the RX64DTH architecture is discussed in detail. The layout of the IC is presented in Section III and the test board is described in Section IV. The measurement results are discussed in Section V. Summary of the IC performance is provided in Section VI.

II. RX64DTH Architecture

The architecture of RX64DTH follows the concept of a binary readout of the previous RX64 integrated circuit optimized to the low amplitude input signals for diffractometry application (X-ray of energy 8 keV deposited in SSD) [6], [7]. The main functional extension is to use two discriminators per channel, with the possibility of counting pulses which are above the low and high thresholds independently. This feature allows one to profit from spectrometric properties of the SSD. The requirements of medical imaging to work with the higher X-ray energy (in our case up to 44 keV) forced us to completely redesign the RX64 chip, and implement in RX64DTH some new solutions, which make the parameters of the ASIC adequate for the foreseen applications. As the multichannel ASIC design is concerned the above mentioned improvements require:

- — careful noise optimization; though the amplitudes of the input signals are large nevertheless we aim to distinguish between pulses of amplitudes which are close to each other (e.g., pulses generated by X-rays of 31 and 35 keV),
- — a new structure of $\mathrm{CR}\text{-}(\mathrm{RC})^2$ shaper amplifier with the low power dissipation and good gain uniformity,
- — the design of a pair of discriminators for each channel, having in mind the low spread of offsets, problems with the switching noise (both comparators work simultaneously), and required linear range for the input signals,

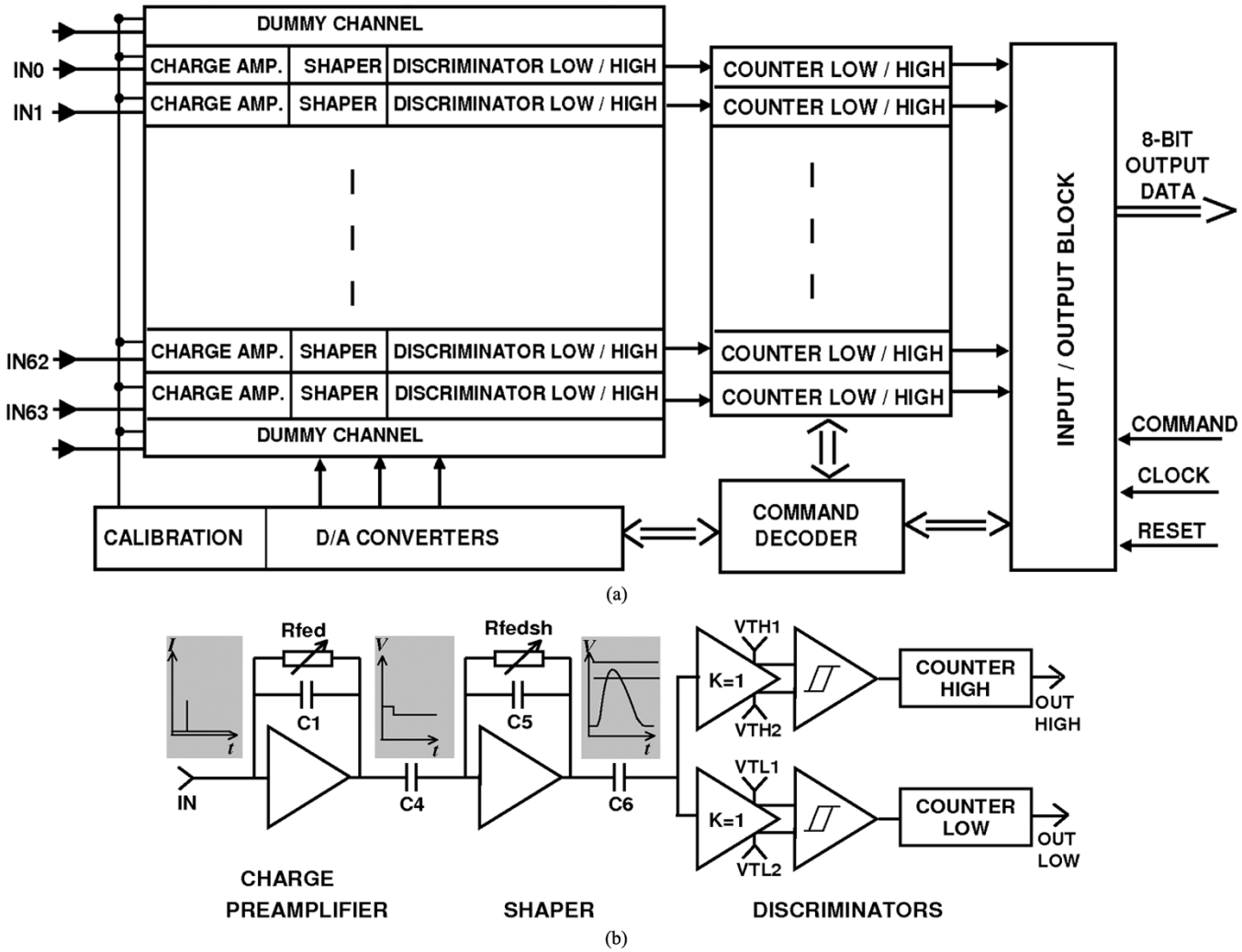

Fig. 1. (a) Block diagram of RX64DTH IC, (b) block diagram of single channel.

— an increase of the functionality and testability of ASICs to make them flexible in systems comprising several hundreds of channels or more.

The above mentioned aspects of the RX64DTH design like the low level of noise, good matching performance from channel to channel, minimization of the switching noise and low power dissipation are known to the community of electronic VLSI designers, but it is also known that in a complex multichannel system they often impose contradictory requirements.

A. Block Diagram of RX64DTH

The block diagram of RX64DTH IC is shown in Fig. 1(a). The ASIC consists of six basic blocks: 64 analog front-end channels, 2×64 counters, an input-output (I/O) block, a command decoder, digital to analog converters and a calibration circuit. The block diagram of a single analog channel is shown in Fig. 1(b). Each channel contains a charge sensitive preamplifier, a shaper, two independent discriminators and two independent 20-bit counters. The charge preamplifier integrates the current input signal from a SSD and gives the output voltage step signal with an amplitude proportional to the total charge generated in the detector. The shaper circuit provides noise filtering and semi-Gaussian pulse shaping with the possibility of the continuous peaking time control in the range from 0.5 to 1 μs. Each front-end channel is equipped with two discriminators which are set for low and high threshold respectively. Pulses above the low and above the high threshold are counted independently by a pair of counters placed in every channel. The data from both counters in each channel are sent outside the ASIC to a digital I/O acquisition card on a personal computer and then analyzed.

B. Noise Optimization of the Preamplifier

The charge preamplifier is based on folded cascode configuration (transistors M1–M4, see Fig. 2) with a feedback loop made of the capacitor C_1 of 200 fF and transistor M5 working in a linear region. The source follower M6–M7 is added to provide the capability for driving the following shaper stage. In response to a δ-like current pulse carrying charge Q, a voltage step of amplitude Q/C_1 is produced at the charge preamplifier output. This voltage step is applied to a bandpass filter CR-$(\mathrm{RC})^2$ with the following time constants:

$$\tau_d \approx \frac{C_2\,(C_{os} + C_3)}{g_{m13} C_3} \tag{1}$$

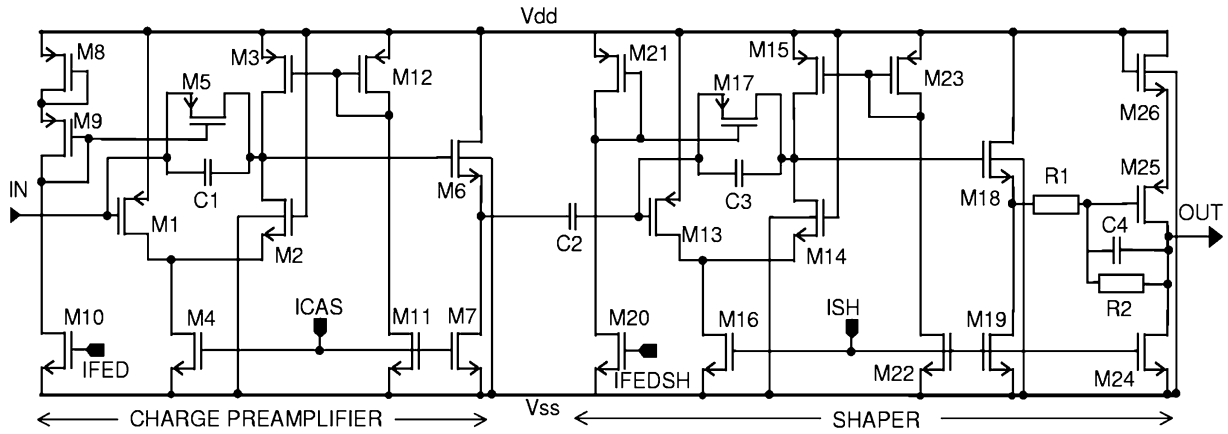

Fig. 2. Schematic diagram of the charge preamplifier and shaper.

$$\tau_{i1} \approx r_{ds17} C_3 \tag{2}$$

$$\tau_{i2} \approx R_2 C_4 \tag{3}$$

where C_{os} is the capacitance to ground seen from the drain of transistor M15, g_{m13} is the transconductance of M13, and r_{ds17} is the drain-source resistance of M17. The bias currents in the shaper are controlled via the current mirrors by the reference currents IFEDSH and ISH. This solution offers the possibility to control the r_{ds17} and g_{m13} and in this way the time constants τ_{i1} and τ_d.

The noise optimization of this stage, for a given detector capacitance and leakage current, can be found in many papers [8], [9] which consider mainly noise contributions from the input transistor and feedback resistance. For the circuit shown in Fig. 2 the noise optimization was based on the assumption that the maximum allowable power dissipation in the preamplifier and shaper together should be about 2 mW. During detailed studies, we concluded that in the proposed design for the interesting range of peaking time the following four elements of the charge preamplifier contribute to the noise:

- — input transistor M1 ($W_1/L_1 = 500\ \mu\mathrm{m}/1\ \mu\mathrm{m}$, with transconductance $g_{m1} = 4.2\ \mathrm{mA/V}$ for drain current of 500 μA),
- — transistor M5, which works in feedback as high value resistor ($W_5/L_5 = 2\ \mu\mathrm{m}/120\ \mu\mathrm{m}$, with the possibility of r_{ds5} control in the range from tens to a hundred MΩ),
- — current source $\mathrm{M4}(W_4/L_4 = 100\ \mu\mathrm{m}/10\ \mu\mathrm{m})$,
- — parasitic series resistance r between detector and input transistor M1 (in order of a few tens of ohms).

The small signal parameters of MOS transistors necessary to perform the above optimization, were taken directly from the HSPICE simulation using the BSIM3v3 transistor model (for detailed methodology see [10]). The results of noise simulation for significant noise components versus peaking time are shown in Fig. 3. The simulation was performed for the total input capacitance $C_{in} = 4$ pF, parasitic resistance $r = 40\ \Omega$ and drain-source resistance r_{ds5} equal to 20 MΩ. Relatively high contribution to the equivalent noise charge (ENC) from the feedback transistor M5 can be minimized by setting a higher value of the small drain-source resistance r_{ds5}. However in the case of direct coupling between the preamplifier and detector, the value of leakage current puts limitation on the value of feedback resistance. The actually chosen feedback resistance corresponds to the requirement of providing the leakage current for the worst of 384 strips of the silicon detector used in our test board (we used an ac coupled detector, which had oxide pin-hole problem for several strips [11]).

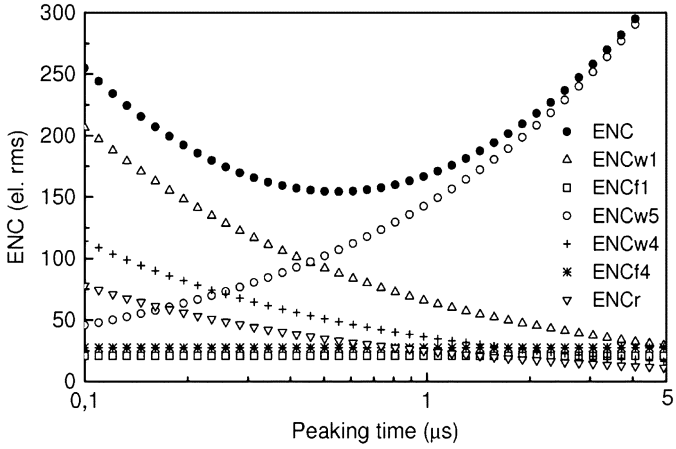

Fig. 3. Contributions of different components in the preamplifier to total ENC versus peaking time: ENC_{w1} channel thermal noise of M1, ENC_{f1} flicker noise of M1, ENC_{w5} channel thermal noise of M5, ENC_{w4} channel thermal noise of M4, ENC_{f4} flicker noise of M4, ENC_r thermal noise of parasitic resistance r.

The flicker noise components of the transistors M1 and M4 are negligible on all peaking time range shown in Fig. 3.

C. Discriminators

To reduce the channel-to-channel offset variation in a large multichannel IC, the discriminators are ac coupled to the shaper and are designed in a fully differential mode (see Fig. 4). In each channel the two discriminators work independently. The input differential stages M27-M31 and M45-M49 have the gain of about 0 dB and are used to provide differential threshold voltages, VTL1-VTL2 for the low and VTH1-VTH2 for the high thresholds. To reduce the effects of offset spread both these stages are biased from a common voltage divider made out of transistors M32-M34. The following stages M35-M43 and M50-M58 work as comparators with hysteresis. The hysteresis is controlled by an external current IDIG. In order to reduce the

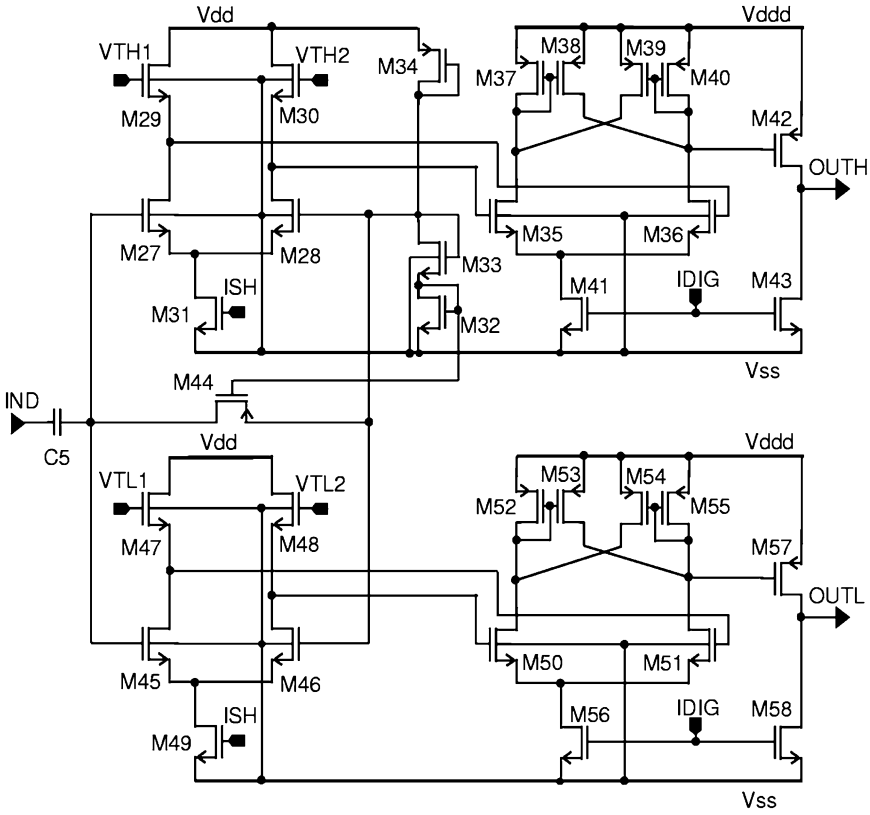

Fig. 4. Schematic diagram of a pair of the discriminators.

effect of the switching of the comparator on the preamplifier and shaper performance, the positive power supply rail *Vdd* is limited to the differential pair, and the separate *Vddd* power rail is used for the comparators.

Taking into account the process matching parameters we sized transistor dimensions to obtain the offset spread less than 1.7 mV rms. This was verified by the Monte Carlo simulation [12].

The obtained range of linearity of the whole front-end chain was up to the input charge of 12 000 electrons, which corresponds to the X-ray energy range (deposited in SSD) up to 44 keV.

D. Counters and Data Outputs

To minimize the silicon area occupied by the counters, their architecture was based on the concept of a pseudorandom shift register [13]. The 20-bit shift register is configured with a single XOR gate to generate a pseudorandom state sequence (see Fig. 5). The 17th and the 20th bit of the shift register are XOR-ed and fed back to the register input, so that the period of the pseudorandom sequence is $2^{20} - 1$.

The operation of the counters is controlled by four signals: *Gate*, *ClkEx*, A/R and *Dest/NonDest*. The *Gate* signal is used to open or close the inputs to the counters. When the inputs are closed, it is possible to set the counters to the readout mode using A/R (*Accumulation/Read*) control line. There are two possible modes of the readout procedure, which are controlled by the *Dest/NonDest* (*Destructive/Non-Destructive*) signal. In the destructive mode all bits in the shift register are set to "1" after reading out the content of the counter, while in the nondestructive mode the configuration of bits in the shift register remains unchanged. The readout of the counters is performed synchronously with the rate determined by the clock signal *ClkEx* applied externally.

A drawback of the scheme based on the pseudorandom shift register is that in order to read out the content of the register one has to stop collecting data. In a continuous experiment this generates a dead time. In order to minimize the dead time, the counters are grouped in the blocks of 16 counters each, and the data from these eight blocks are read out via an 8-bit bus. In order to send the data, sixteen 20-bit shift registers are arranged into a single 320-bit long shift register, and the data can be sent off the ASIC with 10-MHz clock frequency. The data outputs are designed in a standard tri-state single-ended configuration, in order to allow one to connect outputs of several integrated circuits to a common external bus.

E. Testability and Functionality

To increase the RX64DTH functionality and testability we implemented the command decoder, several internal digital-to-analog converters (DACs) and the calibration circuit directly on IC. The command decoder block receives commands in LVDS standard [14] from an external controller (typically a PC I/O card buffered with TTL-LVDS translators) via a serial link, decodes them, and generates signals to the other blocks on the IC. The commands implemented in RX64DTH can be divided into the following three groups:

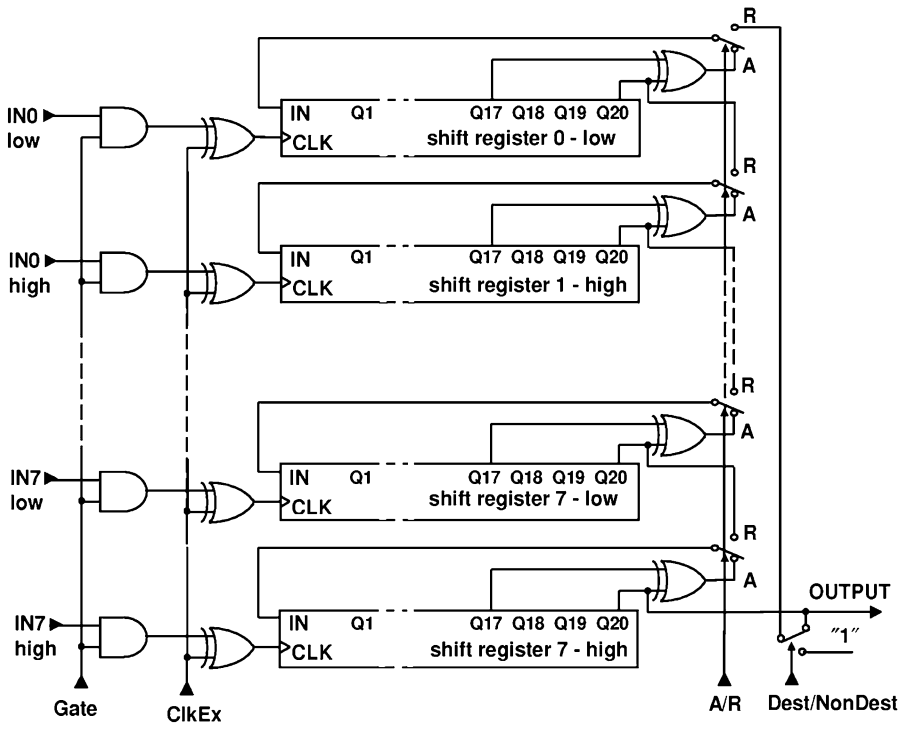

Fig. 5. Simplified block diagram of a group of counters connected to 8 readout channels.

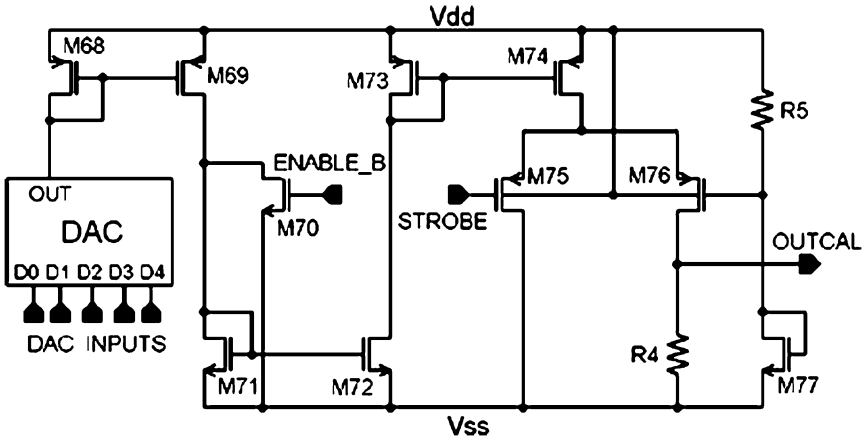

Fig. 6. Schematic diagram of the calibration circuit.

— initialization commands, which load the DACs values to control gain, peaking time and discriminator thresholds;
— normal operation commands, which control the measurement time and data readout;
— test commands, to check the functionality of the counters and the output readout circuit, and to measure analog parameters of the front-end circuit.

The binary architecture implemented in the RX64DTH limits the testing methods which can be used to determine the gain and the noise of the front-end circuit. We calculate these parameters from the distributions of the signal amplitude at the discriminator outputs, which are measured by scanning the threshold of the discriminators for given input signals [7]. The input signals can be obtained directly from the detector (using, e.g., X-ray source) or generated internally on the IC with the calibration circuit. The calibration circuit is connected by small test capacitors $C_t = 75$ fF to the input of each preamplifier. It produces a square wave signal of small amplitude V_t, which applied to the test capacitor generates short current pulses of well controlled charge $Q_{in} = C_t \times V_t$ at the input of the preamplifier.

The main part of the calibration circuit is shown in Fig. 6. In response to the square wave of 4 V amplitude at the STROBE input the circuit generates a square wave at the output, but of small amplitude. The amplitude of the OUTCAL signal is controlled by 5-bit current DAC in the range from 1 mV to 30 mV. The RX64DTH has four calibration circuits, and each of them delivers the test signal to 16 channels simultaneously. The calibration circuit is activated by a low signal at the ENABLE_B input.

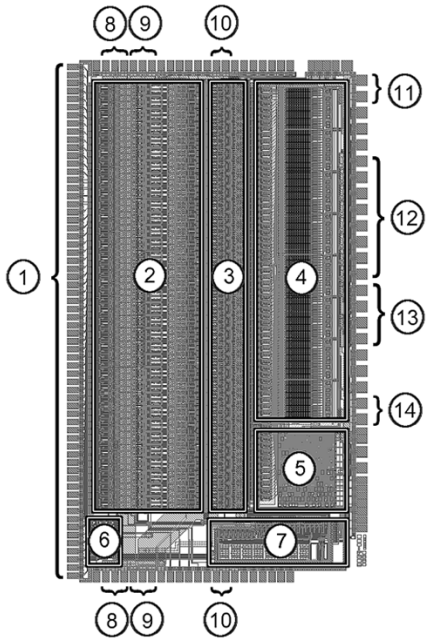

Fig. 7. Layout of the RX64DTH: 1—input pads, 2—charge preamplifiers and shapers, 3—discriminators, 4—counters, 5—command decoder, 6—calibration, 7—DACs, 8—analog power supply (Vdd), 9—analog ground, 10—power supply for discriminators (Vddd), 11—power supply for digital blocks, 12—data output pads, 13—control pads, 14—digital ground.

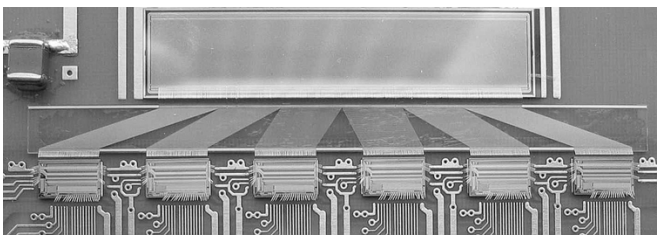

Fig. 8. Fragment of the test board: strip detector and six RX64DTH ICs.

III. Layout Design

The RX64DTH IC was designed in 0.8-μm double-metal, double-poly, n-well CMOS technology process by AMS. The layout of the IC with the major blocks is shown in Fig. 7. The total die area is 3700 μm$\times$ 6500 μm. As the IC contains both analog and digital circuits placed on a common epi-type substrate, particular attention was paid to the floor plan, guard rings and distribution of power supply voltages. The analog and digital blocks have separate bonding pads for their power supply lines. For all critical paths, like power supply lines we calculated parasitic resistances according to their dimensions and then took them into account during post-layout HSPICE simulations.

IV. Test Board

Six RX64DTH ICs were glued on a small printed circuit board (PCB), together with a 400-strip silicon detector (see Fig. 8). The basic detector parameters were: $p+$ strip on n-type substrate of 300 μm thick, strip pitch 100 μm and strip length 1 cm. Detector was of AC coupled type and had field oxide field-effect transistor (FOXFET) bias structure. The detector leakage current was typically below a 100 pA/strip and the total strip capacitance was about 3 pF. This sensor was designed and fabricated by ITC-IRST, Trento, Italy.

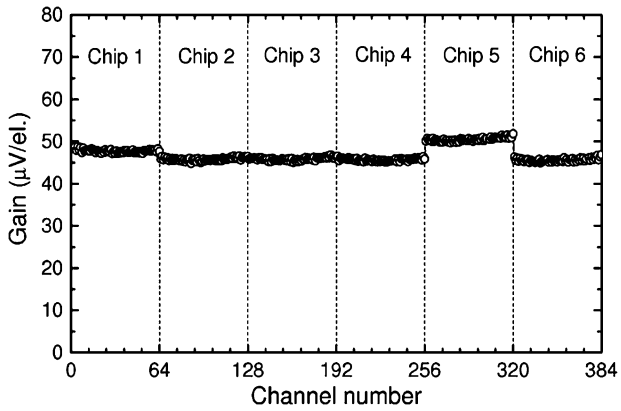

Fig. 9. Spread of gain.

The 384 strips of the silicon detector were connected to 6×64 channels of readout electronics using a pitch adapter printed on glass, and the wire bonding technique. The resistance of a fanout connection was about 35 Ω.

To obtain good detection efficiency the module is to work in edge-on configuration (the strips are oriented parallel to the incoming X-ray beam) [5]. In this configuration a single board is a row of 384 pixels with pitch of 100 μm. To obtain a two-dimensional image, the use of mechanical scan in the direction perpendicular to board plane is planned. A similar approach is also under investigation by several groups working on X-ray medical imaging [15]–[17].

V. Measurement Results

The board was tested using a Cu-anode X-ray tube, with different targets (Ge, Zr, Nb, Mo, Ag, Sn). In this set-up six different values of X-ray energy were available. Scanning discriminator thresholds of the RX64DTH for a given energy of X-ray radiation, one can extract the gain, offset and noise in all 384 channels of readout electronics. To evaluate the performance of the whole system in a real environment the measurements were done simultaneously for all channels. A fixed width of the energy window was set during the measurements (both thresholds were scanned simultaneously). The results are shown in Fig. 9 for the gain, in Fig. 10 for the noise and in Fig. 11 for the offset in the low threshold discriminator.

Table I summarizes the mean values and standard deviations of the above mentioned parameters for each ASIC on the test board.

The effective threshold setting for a given input signal depends both on the gain of single channel and the discriminator offset. It is clearly visible (see Table I) that the spread of analog parameters, e.g., gain from channel to channel inside a single ASIC is smaller than the spread of gain between different dies on the same PCB. To reduce this effect we implemented the possibility of loading different DACs values for setting the gain and discriminator thresholds for each integrated circuit on the board. A local 3-bit address of die was implemented in the command format sent to ASIC. This protocol guarantees the cancellation of an unwanted spread of effective thresholds between ASICs

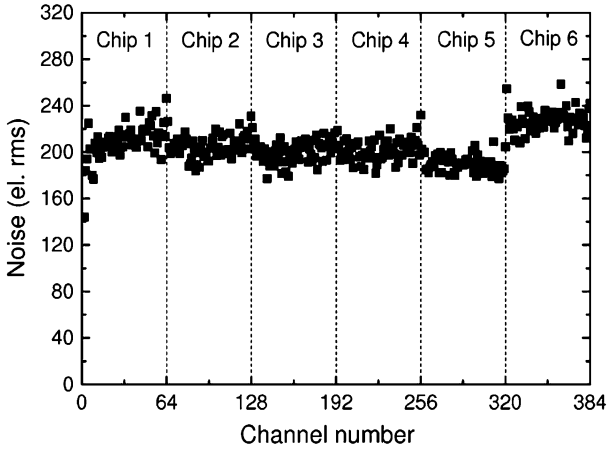

Fig. 10. Spread of noise—data for Ag peak.

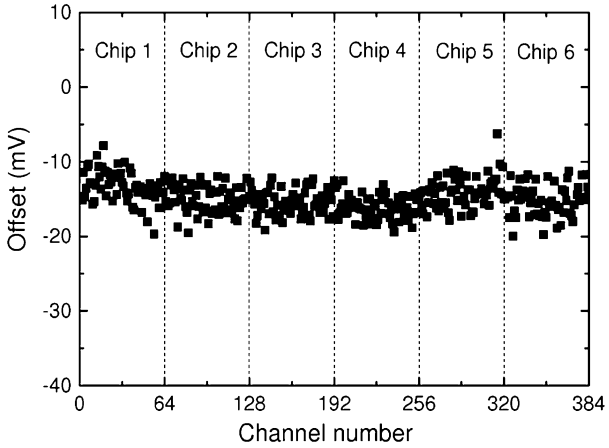

Fig. 11. Spread of offset for low threshold discriminator.

TABLE I
ANALOG PARAMETERS OF SIX RX64DTH ICS INSTALLED ON PCB

Chip number	Gain [μV/el] mean (sd.)	Noise [el. rms] mean (sd.)	Offset-L* [mV] mean (sd.)	Offset-H# [mV] mean (sd.)
1	47.7 (0.37)	209 (15)	-13.3 (2.1)	-13.9 (1.8)
2	45.8 (0.38)	205 (9.5)	-15.0 (1.8)	-15.9 (1.7)
3	45.8 (0.35)	200 (9.3)	-15.5 (1.7)	-16.1 (1.8)
4	45.7 (0.32)	202 (9.4)	-16.1 (1.5)	-16.7 (1.7)
5	50.5 (0.44)	190 (7.2)	-14.0 (2.0)	-15.1 (2.0)
6	45.6 (0.40)	227 (9.6)	-15.2 (2.0)	-15.8 (1.9)

*Offset-L was measured for low threshold discriminator
#Offset-H was measured for high threshold discriminator

on the same PCB with the precision equal to 1 LSB of DAC threshold.

Let us consider the module performance in possible future tests in clinical diagnostics with dual energy of X-ray beams. For example, in coronary angiography medical examinations are aimed at the visualization of coronary arteries with contrast agent injected. The typical contrast medium with iodine has a K-edge absorption at 33.17 keV. The idea is to take images of

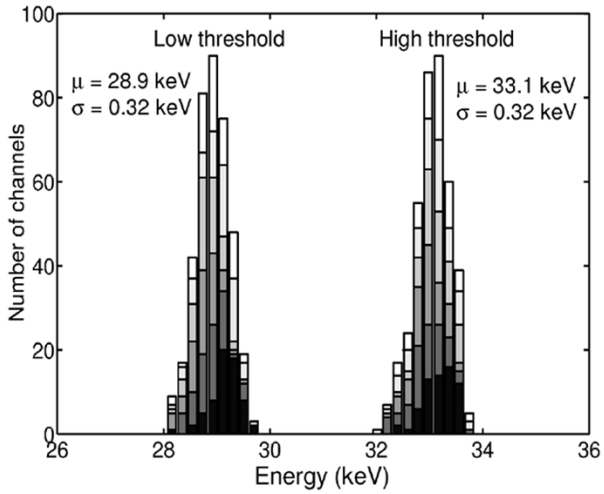

Fig. 12. Spread of the low and high thresholds in 384-channel module used to digital imaging with X-ray beam of dual energy 31 and 35 keV.

TABLE II
SUMMARIZED PERFORMANCE OF RX64DTH IC

Parameter	
Technology	CMOS 0.8 μm
Size	3.7 mm × 6.5 mm
Number of channel	64
Supply voltage	3.5 - 4 V
Power dissipation per channel	4 mW
Peaking time	0.5 –1 μs
ENC (*Tp* = 0.8 μs, *Cdet* = 3 pF)	200 el. rms
Gain	46 μV/el.
Uniformity	
- spread of offset (sd)	1.7 mV
- spread of gain (sd/mean)	0.8%
Communication	
- control	via serial link
- data output	three state 8-bit bus

the tested object at two different values of X-ray energy (31 keV and 35 keV) which are below and above the iodine K-edge, and then to perform (logarithmic) subtraction to extract the iodine signal. To check the electronic readout system performance, we have assumed that the low threshold discriminators should count the photons of both energy values (31 keV and 35 keV) at the same time, while the high threshold discriminator should count only higher energy photons (35 keV).

Taking into account the spreads of analog parameters and the possibility of setting the thresholds in each IC independently, we have calculated the energy threshold spread of this 384-channel system for the above mentioned application. The histogram of threshold spread of six ICs installed on the module (expressed in energy) is shown in Fig. 12. The spread of threshold is equal to 0.32 keV, i.e., 87 el. rms assuming 3.67 eV for the generation of an electron-hole pair in the silicon detector. This spread is much smaller compared with the measured noise $\mathrm{ENC} \approx 200$ el. rms, so the threshold spread does not limit the performance of the system.

The ENC obtained from the measurements is 25% higher than the predicted one by the simulations. This can be attributed to

the following phenomena, which were difficult to take into account during the simulation stage:

— excess noise due to short channel effects [18]–[20];
— substrate noise due to a large number of working digital blocks [21], [22];
— supply bounce noise of the whole 384-channel system [23].

Using the mechanical scanning a question to be answered concerns the high rate operation of the presented ASIC, which is determined in this case by an analog front-end electronics performance. The high rate capability is not a subject of the present study, but a similar front-end was measured in detail for a previous analog version of this integrated circuit giving the rate of 100 kHz per channel for statistically distributed photons from the X-ray tube [24]. Since the circuit solutions in the analog front-end part of electronics and the peaking time in both versions are similar, we do not expect significant difference in counting rate. To reduce an acquisition time during medical imaging we are planning to use several PCBs (like this one in Fig. 8) stacked in parallel and spaced by a few millimeters. This allows one to limit mechanical scanning only to the distance between two PCBs.

VI. Summary

We have presented the RX64DTH IC, which is a fully integrated digital readout for the SSD, and which additionally provides some energy information aboutthe X-ray radiation. The IC performance is summarized in Table II.

The noise and matching measurements of multichannel test board show that RX64DTH ICs can be used to build a medical imaging system for dual energy mammography, coronary angiography or bone densitometry. Examples of using the above described multichannel system for taking the images of mammographic phantoms are presented in [5].

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